DATA SHEET

TDA8579
Dual common-mode rejection differential line receiver

Product specification
Supersedes data of January 1994
File under Integrated Circuits, IC01

1995 Dec 15

Philips
Semiconductors

PHILIPS

Dual common-mode rejection differential line receiver

TDA8579

FEATURES

- Excellent common-mode rejection, up to high frequencies
- Elimination of source resistance dependency in the common-mode rejection
- Few external components
- High supply voltage ripple rejection
- Low noise
- Low distortion
- All pins protected against electrostatic discharge
- AC and DC short-circuit safe to ground and V_{CC}
- Fast DC settling.

GENERAL DESCRIPTION

The TDA8579 is a two channel differential amplifier with 0 dB gain and low distortion. The device has been primarily developed for car radio applications where long connections between signal sources and amplifiers (or boosters) are necessary and where ground noise has to be eliminated. The device is intended to be used to receive line inputs in audio applications that require a high level of common-mode rejection. The device is contained in an 8-pin small outline (SO) or dual in-line (DIP) package.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		5.0	8.5	18	V
I_{CC}	supply current	V_{CC} = 8.5 V	–	11	14	mA
G_v	voltage gain		–0.5	0	+0.5	dB
SVRR	supply voltage ripple rejection		55	60	–	dB
V_{no}	noise output voltage		–	3.7	5.0	μV
$\lvert Z_i \rvert$	input impedance		100	240	–	kΩ
CMRR	common-mode rejection ratio	R_s = 0 Ω	–	80	–	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8579	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1
TDA8579T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

Dual common-mode rejection differential line receiver

TDA8579

BLOCK DIAGRAM

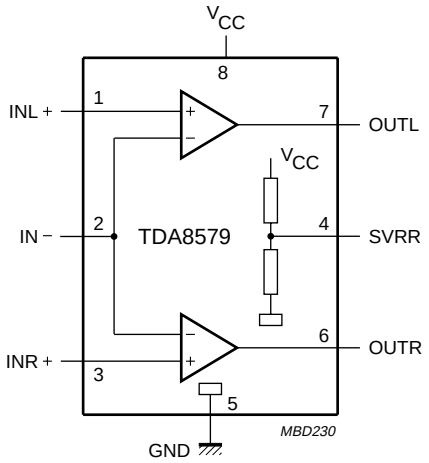


Fig.1 Block diagram.

FUNCTIONAL DESCRIPTION

The TDA8579 contains two identical differential amplifiers with a voltage gain of 0 dB. The device is intended to receive line input signals for audio applications. The TDA8579 has a very high level of common-mode rejection and thus eliminates ground noise. The common-mode rejection remains constant up to high frequencies (the amplifier gain is fixed at 0 dB). The inputs have a high input impedance. The output stage is a class AB stage with a low output impedance. For a large common-mode rejection, also at low frequencies, an electrolytic capacitor connected to the negative input is advised. Because the input impedance is relatively high, this results in a large settling time of the DC input voltage. Therefore a quick-charge circuit is included to charge the input capacitor within 0.2 seconds.

All input and output pins are protected against high electrostatic discharge conditions (4000 V, 150 pF, 150 Ω).

PINNING

SYMBOL	PIN	DESCRIPTION
INL+	1	positive input left
IN–	2	common negative input
INR+	3	positive input right
SVRR	4	half supply voltage
GND	5	ground
OUTR	6	output right
OUTL	7	output left
V_{CC}	8	supply voltage

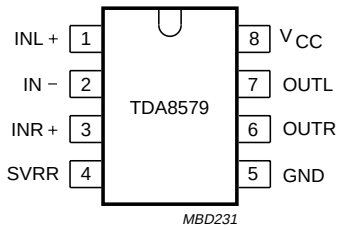


Fig.2 Pin configuration.

LIMITING VALUES

in accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage	operating	–	18	V
I_{ORM}	repetitive peak output current		–	40	mA
V_{sc}	AC and DC short-circuit safe voltage		–	18	V
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	operating ambient temperature		–40	+85	°C
T_j	maximum junction temperature		–	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	TDA8579 (DIP8)	110	K/W
	TDA8579T (SO8)	160	K/W

CHARACTERISTICS

V_{CC} = 8.5 V; T_{amb} = 25 °C; f = 1 kHz; measured in test circuit of Fig.3; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		5.0	8.5	18	V
I_{CC}	supply current		–	11	14	mA
V_O	DC output voltage	note 1	–	4.3	–	V
t_{set}	DC input voltage settling time		–	0.2	–	s
G_v	voltage gain		–0.5	0	+0.5	dB
α_{cs}	channel separation	R_s = 5 kΩ	70	80	–	dB
$\lvert\Delta G_v\rvert$	channel unbalance		–	–	0.5	dB
f_L	low frequency roll-off	–1 dB; note 2	20	–	–	Hz
f_H	high frequency roll-off	–1 dB	20	–	–	kHz
$\lvert Z_i\rvert$	input impedance		100	240	–	kΩ
$\lvert Z_o\rvert$	output impedance		–	–	10	Ω
$V_{i(max)}$	maximum input voltage	THD = 1%	–	2.0	–	V
V_{no}	noise output voltage	R_s = 0 Ω; note 3	–	3.7	5.0	μV
$V_{CM(rms)}$	common-mode input voltage (RMS value)		–	–	1.0	V
CMRR	common-mode rejection ratio	R_s = 5 kΩ	66	70	–	dB
		R_s = 0 Ω; note 4	–	80	–	dB
SVRR	supply voltage ripple rejection	note 5	55	65	–	dB
		note 6	–	60	–	dB
THD	total harmonic distortion	V_i = 1 V;	–	0.02	–	%
		V_i = 1 V; f = 20 Hz to 20 kHz	–	–	0.1	%
THD_{max}	total harmonic distortion at maximum output current	V_i = 1 V; R_L = 150 Ω	–	–	1	%

Notes

1. The DC output voltage with respect to ground is approximately $0.5V_{CC}$.
2. The frequency response is externally fixed by the input coupling capacitors.
3. The noise output voltage is measured in a bandwidth of 20 Hz to 20 kHz (unweighted).
4. The common-mode rejection ratio is measured at the output with a voltage source 1 V (RMS) in accordance with the test circuit (see Fig.3) while V_{INL} and V_{INR} are short-circuited. Frequencies between 100 Hz and 100 kHz.
5. The ripple rejection is measured at the output, with R_s = 2 kΩ, f = 1 kHz and a ripple amplitude of 2 V (p-p).
6. The ripple rejection is measured at the output, with R_s = 0 to 2 kΩ, f = 100 Hz to 20 kHz and a maximum ripple amplitude of 2 V (p-p).

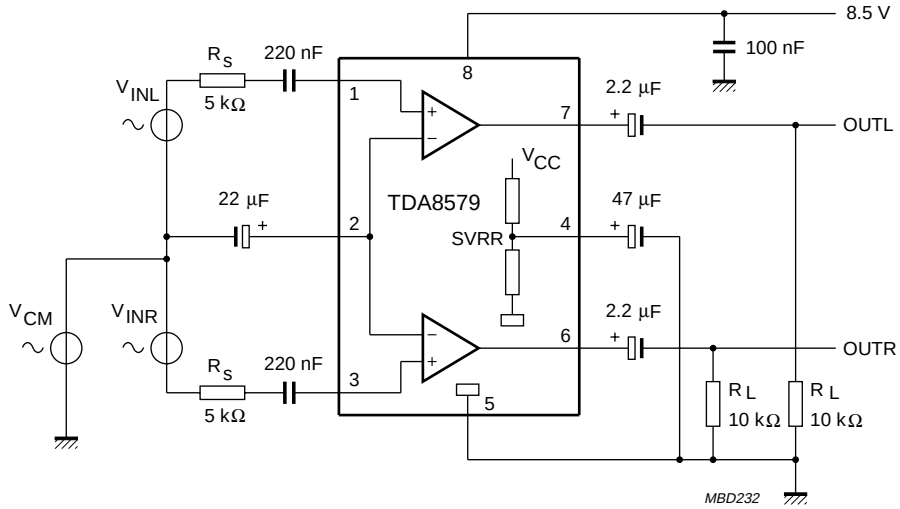


Fig.3 Test and application circuit.

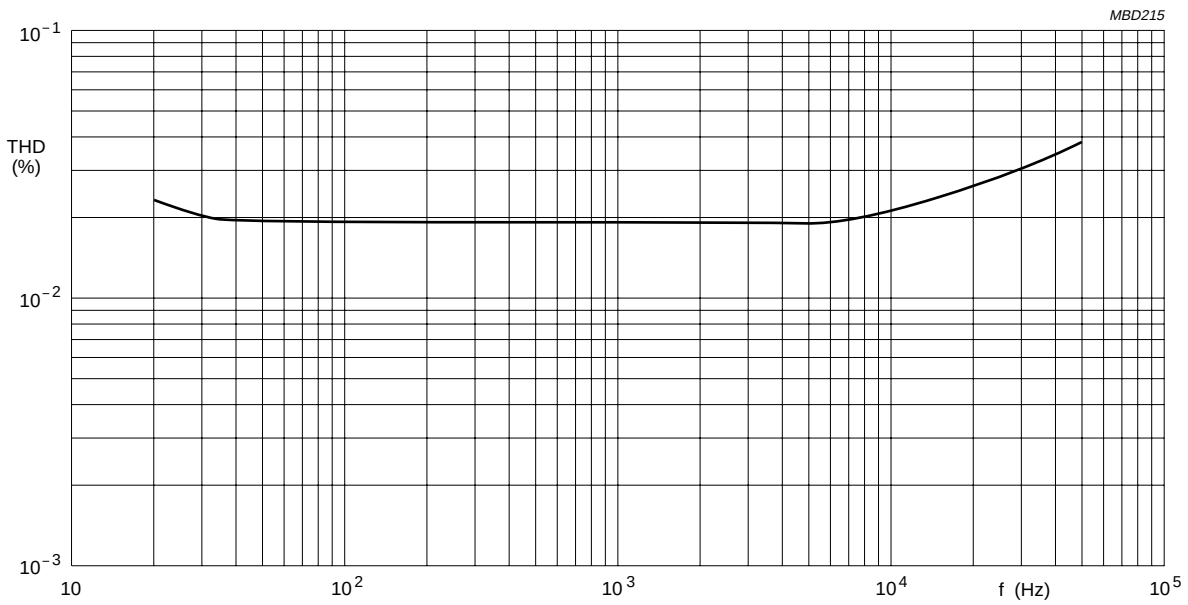
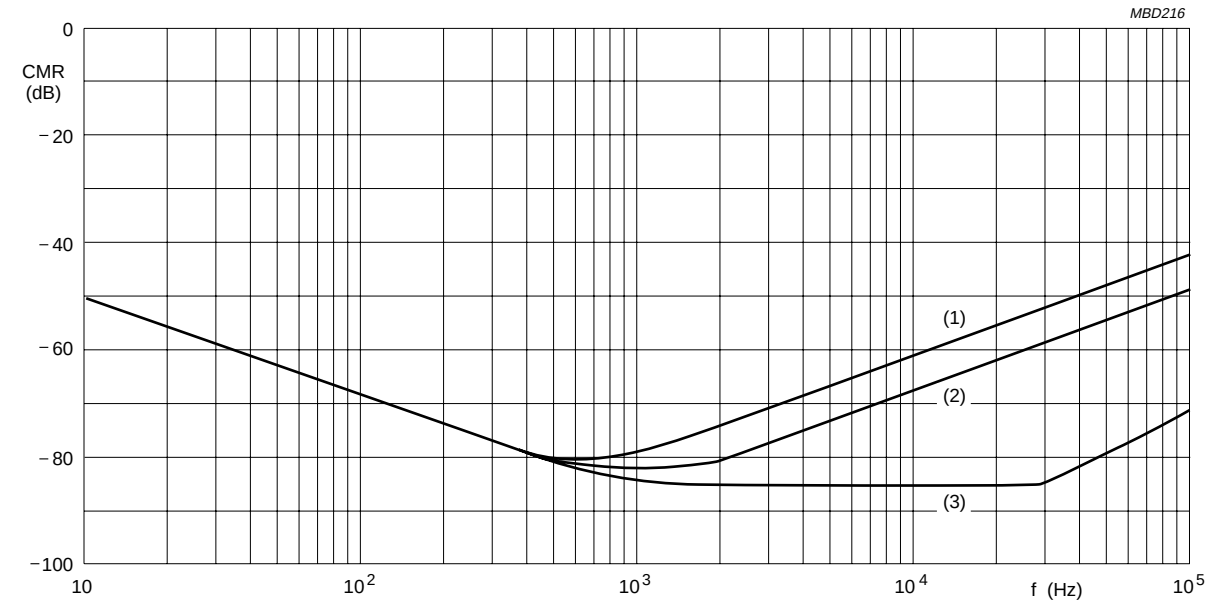


Fig.4 Total harmonic distortion as a function of frequency; V_i = 1 V (RMS).



(1) R_S = 5 kΩ.
(2) R_S = 2 kΩ.
(3) R_S = 0 kΩ.

Fig.5 Common-mode rejection ratio as a function of frequency; V_{CM} = 1 V (RMS).

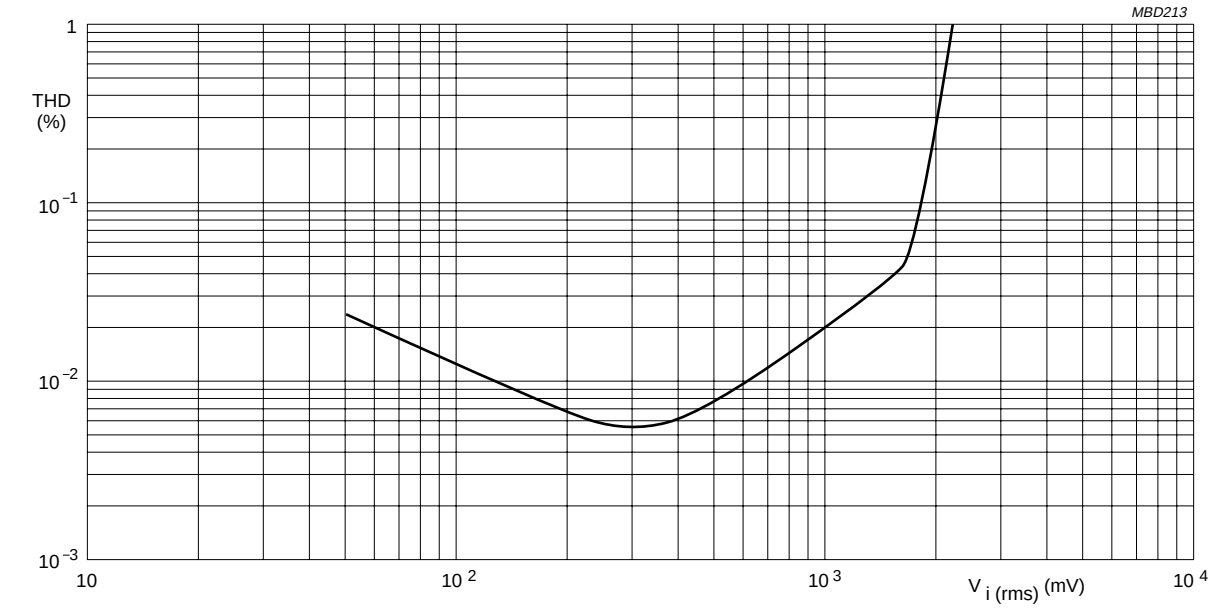


Fig.6 Total harmonic distortion as a function of input voltage; f = 1 kHz.

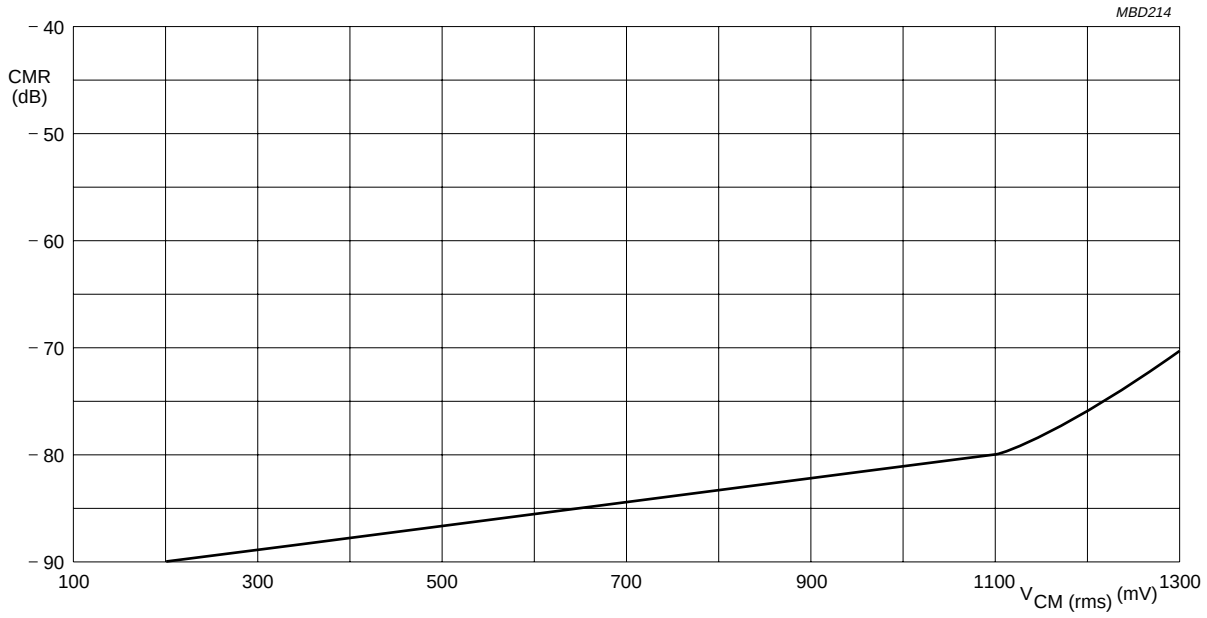
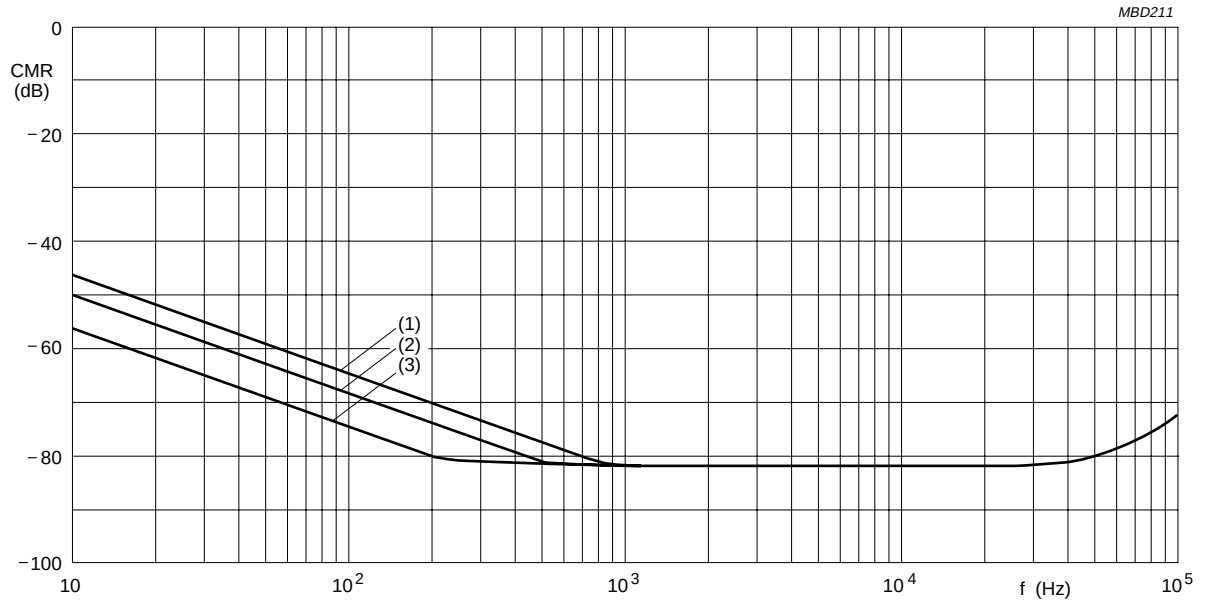


Fig.7 Common-mode rejection ratio as a function of common-mode input voltage; f = 1 kHz (R_s = 0 Ω).



(1) C2 = 22 µF.
(2) C2 = 47 µF.
(3) C2 = 100 µF.

Fig.8 Common-mode rejection ratio as a function of frequency; V_{CM} = 1 V (RMS).

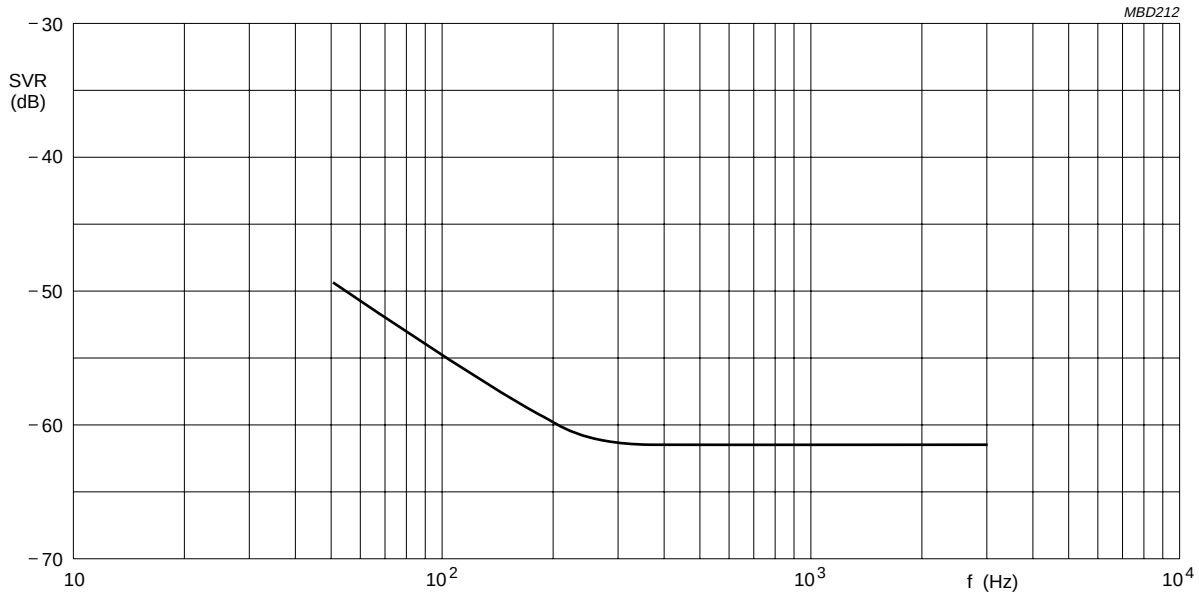
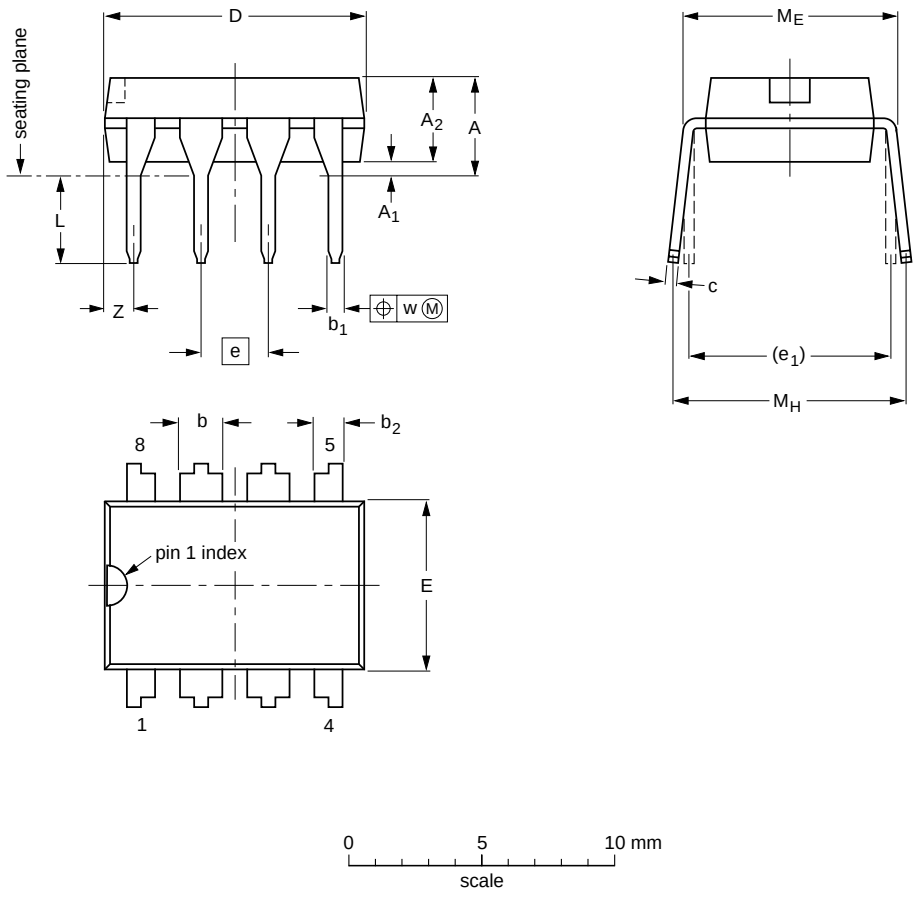


Fig.9 Supply voltage ripple rejection as a function of frequency; V_{ripple} = 2 V (p-p), R_s = 2 kΩ.

PACKAGE OUTLINES

DIP8: plastic dual in-line package; 8 leads (300 mil) **SOT97-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

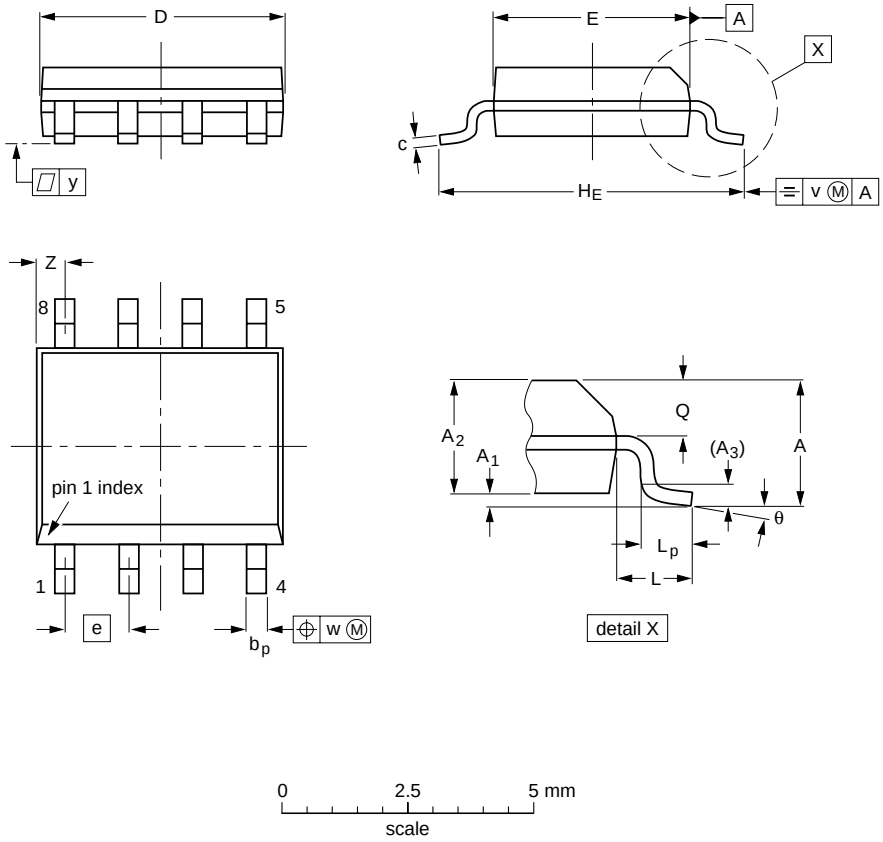
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.14	0.53 0.38	1.07 0.89	0.36 0.23	9.8 9.2	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	1.15
inches	0.17	0.020	0.13	0.068 0.045	0.021 0.015	0.042 0.035	0.014 0.009	0.39 0.36	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.045

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT97-1	050G01	MO-001AN				~~92-11-17~~ 95-02-04

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03S	MS-012AA				~~95-02-04~~ 97-05-22

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

DIP

SOLDERING BY DIPPING OR BY WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

SO

REFLOW SOLDERING

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

WAVE SOLDERING

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

REPAIRING SOLDERED JOINTS

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.