Electronic ballast controller circuit NE5565

DESCRIPTION

The Electronic Ballast controller chip has been designed in a bipolar process. It is housed in a 20-lead dual-in-line plastic package. The control chip contains the equivalent of two (2) switched mode power supply control circuits. The first SMPS controller is a DC-to-DC converter operating in the discontinuous current conduction mode. It is used as a PFC in the ballast system to provide a DC voltage step-up function, good AC power factor, low AC current harmonic distortion, and circuit protection against some types of AC voltage transients. The PFC uses pulse width modulation to control the power transfer with an external MOS power transistor. The second SMPS circuit is a half-bridge oscillator circuit. It converts the DC output voltage of the PFC into a high frequency AC voltage for operating lamps. Power transfer in this circuit is controlled by changing the switch frequency. The half-bridge controller circuit is capable of driving two external high voltage MOS power transistors and it has circuits to regulate the lamp current, limit the peak lamp voltage, and protect the power switches during fault conditions. This electronic ballast controller circuit has the capability of being used in a dimming application.

PIN CONFIGURATION

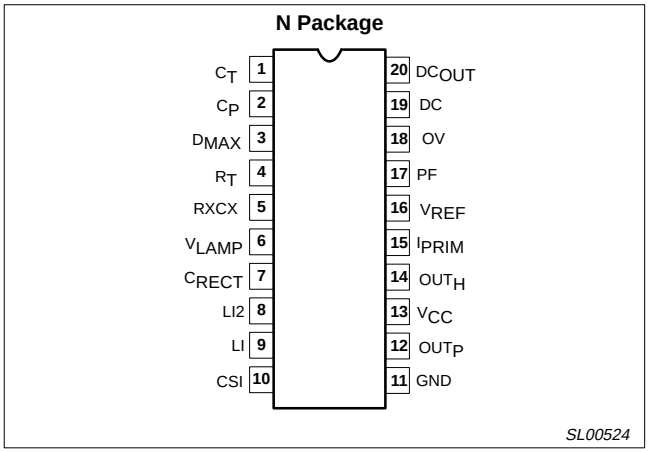


Figure 1. Pin Configuration

FEATURES:

- Complete PFC correction and dimming ballast control on one IC
- Low line current distortion PFC
- Selectable variable frequency modes
- Programmable pre-hit and ignition
- Lamp over-voltage protection
- PFC over-voltage protection for preventing over-shooting due to load removal

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Dual-In-Line Package (DIP)	0 to +85°C	NE5565N	SOT146-1

BLOCK DIAGRAM

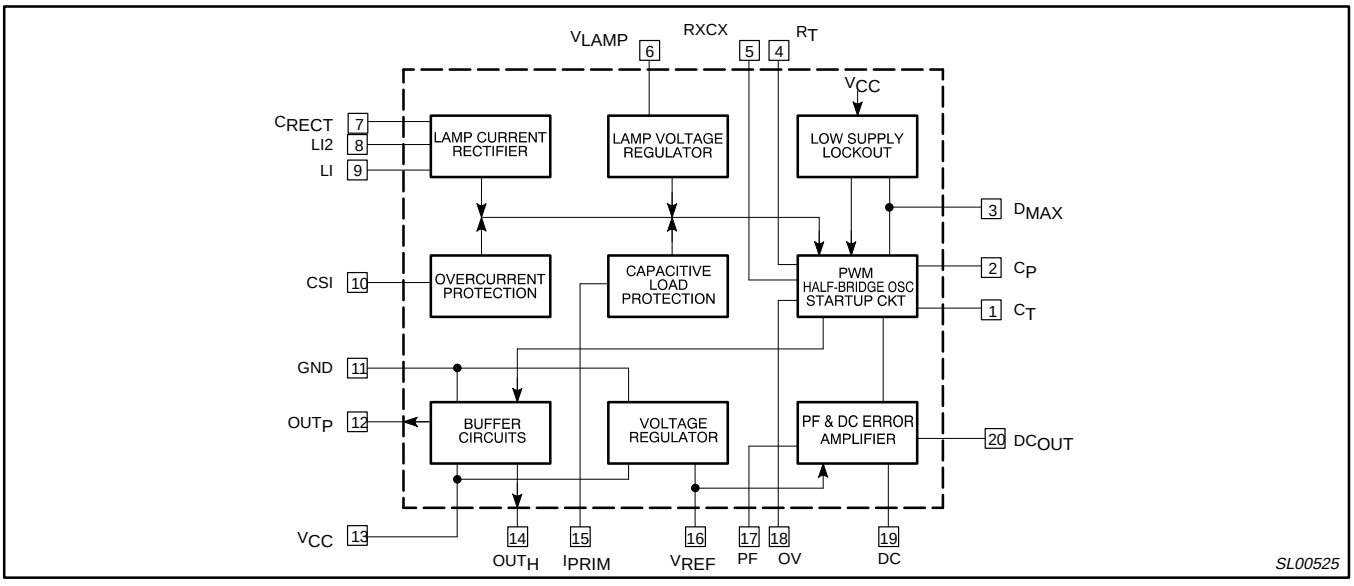


Figure 2. Block Diagram

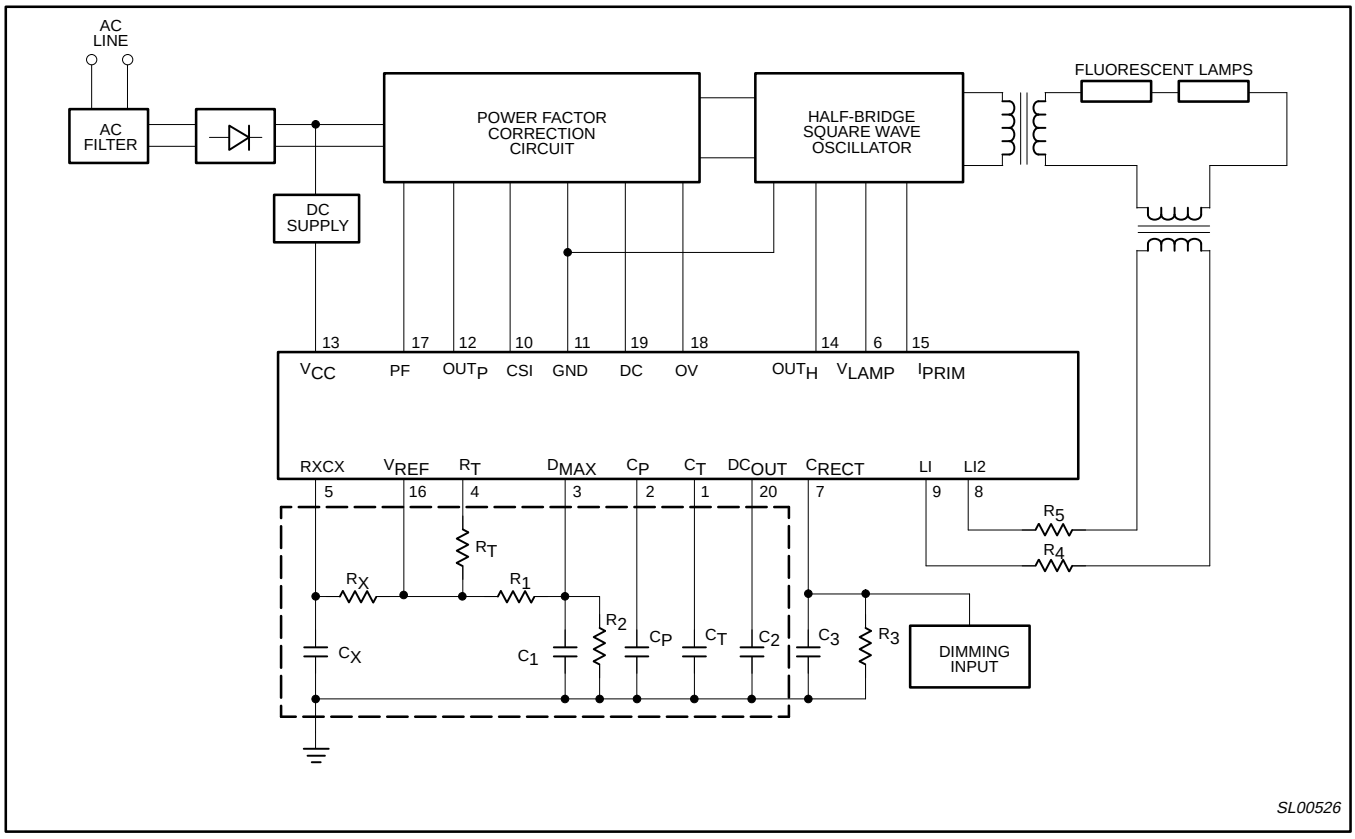


Figure 3. Typical Application: 2-Lamps Dimming Ballast

Voltage Regulator

The V_{REF} output provides a regulated output voltage of 7.42V at the V_{REF} pin. This voltage is used as a reference as well as the power supply of the control logic. It is based on a trimmed band gap voltage reference circuit. The nominal V_{CC} voltage for the control chip is 12.7V. The V_{REF} circuit requires a minimum of 9.3V before it can produce regulated output. The V_{REF} output voltage has an absolute accuracy of ±3.5% over the temperature range of 0°C to 85°C.

Lamp Voltage Regulator

Limits the maximum open circuit voltage across the lamp load during the pre-heat, ignition and lamp removal conditions. During steady state operation, the lamp voltage is governed by the arc voltage of the lamps, not by the control circuit. The lamp voltage comparator is used to sense when the voltage at the V_{LAMP} pin exceeds V_{REF}. At the time this occurs, the lamp voltage has reached its maximum allowed open circuit value and the circuit responds by producing a rapid frequency increase which reduces the voltage at the Vlamp pin. The RxCx time constant sets the frequency sweep time of the start up circuit. The frequency sweep range has a rate of 2:1.

Low Supply Lock-out Protection

Senses the DC power supply voltage at the V_{CC} pin to determine when the PFC and half-bridge control circuits should turn on or off. This protection circuit uses a Schmitt trigger with a voltage reference to determine the upper and lower trip points of the power supply voltage. As the power supply voltage rises from 0V to a value just below the upper trip point of 11V, both the PFC and the half-bridge control circuits are held in the off state. Once the V_{CC} voltage rises above the upper trip point, both PFC and half-bridge oscillator circuits become operational. When the V_{CC} falls below the lower trip point of 10V, both PFC and half-bridge circuits are disabled. Once the half-bridge oscillator turns off, it is not allowed to turn back on until V_{CC} exceeds the upper trip point and a minimum time delay, set by external components at the D_{MAX} pin, has passed.

Start up Ckt

The Low Half-bridge Voltage Lock-out Circuit senses the DC output voltage of the PFC SMPS clrcuit. It is used to inhibit the lamp ignition sequence or frequency sweep of the half-bridge oscillator until the PFC output voltage has reached a pre-determined value. This value is set by external components. The PFC voltage is sensed by the over voltage input pin, OV. When this input exceeds 5/7 of V_{REF} the frequency sweep is allowed to occur, thus beginning the lamp ignition sequence.

The Over Voltage Protection Circuit prevents the PFC DC output voltage from exceeding a pre-determined value. When the voltage at the OV pin is greater than V_{REF} the PFC buffer gate drive output OUT_P is turned off. This prevents any further increase in PFC DC output voltage. The over voltage circuit only protects against an over voltage or over shoot generated by the PFC itself. This may occur during turn on when the SMPS is not loaded and the circuit is under damped. Transient voltages from the AC line are not suppressed by this circuit.

Capacitive Load Protection

Prevents failure of the half-bridge power transistors during lamp removal. It does this by limiting the operation of the half-bridge oscillator to frequencies above the resonant frequency of an

external LC network driven by the bridge. At frequencies above resonance the primary voltage of the half-bridge LC load network leads the primary current in phase. The protection logic senses the LC network current phase relative to the half-bridge gate drive voltage to determine if a resonant condition exists. The Iprim input voltage represents the primary current signal from the external LC network. If the voltage at Iprim is more positive than -100mV when the gate drive signal is high, then a fault condition exists and the half-bridge oscillator frequency is swept high.

Half-Bridge Oscillator

Is a triangle wave generator used to produce a square wave signal for driving the half-bridge buffer circuit. The triangle wave appears on the C_t capacitor output pin. The oscillator frequency is governed by the value of the resistor connected to the R_t input and the value of the C_t capacitor.

Output Buffer Drive

Convert the low level logic signals from the half-bridge oscillator and pulse width modulator into a 10V drive signal for the power switches. The OUT_H half-bridge buffer/drive circuit will drive an external level shift scheme which will then be used to operate the half-bridge power switches. The OUT_P output may directly drive a power MOSFET switch or an external level shift/power MOSFET combination.

Pulse Width Modulator

Generates a ramp voltage used to control the duty cycle of the PFC SMPS. The frequency of the pulse width modulator is set by the half-bridge oscillator. The ramp voltage appears at the C_P output. It is synchronized to the half-bridge oscillator so that the beginning of the ramp occurs at the valley of the C_t triangle waveform. When the ramp voltage at C_P exceeds the voltage at the DC out pin in the DC amplifier, the capacitor connected to C_P is discharged. The period of the PFC gate drive pulse correspond to the C_P ramp time. The maximum duty cycle, soft start function, and half-bridge off time are all controlled by the external capacitor and resistors connected to the D_{MAX} pin.

Over Current Protection

An over current is sensed by an external resistor connected to the current sense input pin, CSl. A voltage of minus 500mV at CSl triggers the over current protection circuit this turns off the OUT_P output and forces the external capacitor connected to D_{MAX} to discharge when an over current condition occurs in the PFC input circuit. An over current condition is usually produced during the turn on transient of the SMPS or when the AC line voltage has a power interruption.

Power Factor Amplifier

Senses the phase and amplitude of a peak rectified AC line voltage in order to modulate the duty cycle of the PFC power switch. This is done to improve the sinusoidal wave shape of the AC line current. The power factor input is provided by the PF input pin. The voltage at this pin is 1V when the AC line voltage reaches its peak and 0V when the AC voltage is at its 0V crossing.

DC Error Amplifier

Provides negative feedback control of the PFC DC output voltage. The DC pin senses the DC output voltage of the PFC through an external resistor voltage divider and filter network. The reference voltage for the DC error amplifier is V_{REF}. The output of the amplifier is available at the DC out pin and an external capacitor is connected to this pin in order to remove switching frequency noise before its signal is applied to the pulse width modulator in the PWM oscillator circuit.

Lamp Current Rectifier

Is used to provide negative feedback control of the average lamp current. An external lamp current transformer and load resistor are used to convert the lamp current signal into a voltage. This voltage is applied to the lamp current input pins, Li1 and Li2. The full wave rectified output is provided at C_{RECT} pin. External resistors and a capacitor determine the gain and time constant of the circuit. A differential error amplifier compares the voltage of C_{RECT} to an internal reference of 2/7 V_{REF} and adjusts the half-bridge oscillator frequency so that the error voltage is minimized. This forces the average lamp current to be a constant.

Dimming

Dimming input should be an extra current put into charging C_3 in addition to the current from Pin 7. This creates the same condition as higher voltage differential across Pins 8 and 9, hence, the IC reacts as if there is too much power applied to the lamps.

PIN DESCRIPTIONS/ABSOLUTE MAXIMUM RATINGS

Pin #	Name	Function	Rating	Units
1	C_t	Half-Bridge oscillator capacitor	7	V
2	C_P	PWM Capacitor for power factor correction circuit	7	V
3	D_{MAX}	Max Duty Cycle, soft start, and time delay R/C input	7	V
4	R_t	Resistor for setting the half-bridge frequency	±0.7V or 500µA	V/µA
5	RxCx	Start resistor and capacitor input for setting frequency sweep time	7	V
6	V_{LAMP}	Lamp voltage regulator input	14	V
7	C_{RECT}	Lamp current rectifier capacitor input/dimming control input	7	V
8	Li2	Lamp current differential inputs	±1V to Li1, 7V or V_{REF} -0.7V to GND	V
9	Li1			
10	CSl	Current sense input for over-current protection	+0.5 V / -2V	V
11	GND	Ground	0	V
12	OUT_P	Gate drive output for the PFC	14	V
13	V_{CC}	Positive power supply voltage	14	V
14	OUT_H	Gate drive output for the half-bridge DMOS	14	V
15	I_{PRIM}	Primary current sense input	+1V / -1.5 V or ±500µA	V/µA
16	V_{REF}	Regulated output voltage and reference	V_{CC}	V
17	PF	Power factor input	7	V
18	OV	0ver-voltage comparator input	14	V
19	DC	DC error amplifier input	12	V
20	DC_{OUT}	DC error amplifier output for connecting to external filter capacitor	7	V

DC ELECTRICAL CHARACTERISTICS

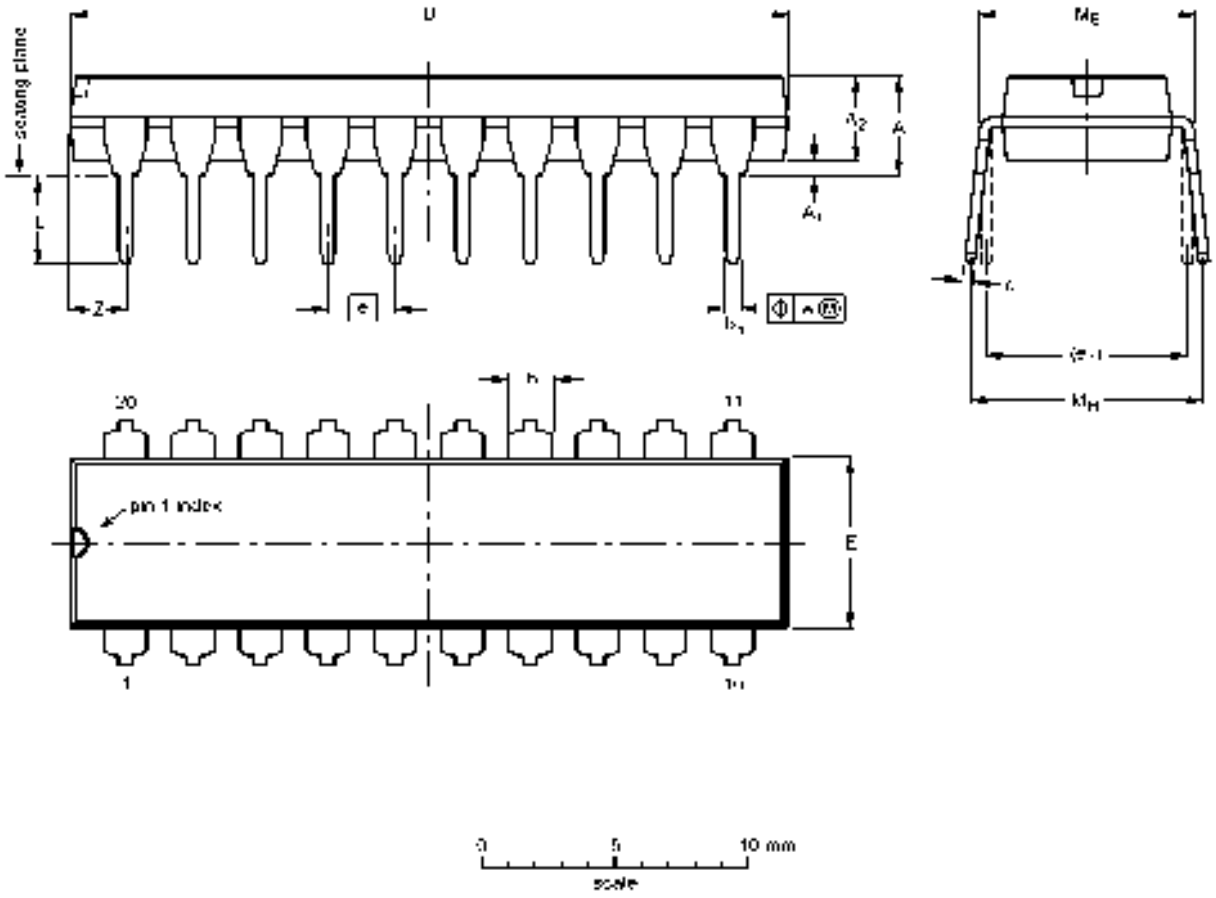
V_{CC} = +12.7V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
DC Error Amplifier						
	DC input clamp current	DC = 0V	-403	-690	-941	µA
	DC bias current	DC = V_{REF}			-1	µA
	DC error amp reference		7.05	7.42	7.79	V
	DC output HIGH voltage	DC = 7V	5.4		6.6	V
Power Factor Amplifier						
	PF input current	PF = 1V			-14	µA
	PF transconductance		65	100	135	µA/V
Start-up Circuit						
	RxCx input current	RxCx = 0.5V			-8	µA
	RxCx threshold		1.51	1.59	1.67	V
	OV input current	OV = 5V			-8	µA
	OV threshold		7.05	7.42	7.79	V
	HB lockout threshold		4.93	5.3	5.67	V
Oscillator						
	R_t voltage			.7		V
	C_t HIGH current	RxCx=0V Rt=100µA	-160	-200	-240	µA
	C_t LOW current	RxCx=6.5V Rt=100µA	-80	-100	-120	µA
	C_t HIGH threshold		4.14	4.6	5.06	V
	C_t LOW threshold		2.23	2.48	2.73	V
PWM						
	C_P HIGH threshold		3.66	4.07	4.48	V
	C_P-to-D_{MAX} threshold	D_{MAX} = 4V	2.97	3.3	3.63	V
	C_P-to-DC output threshold	DC = 4V	2.97	3.3	3.63	V

DC ELECTRICAL CHARACTERISTICS (continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
PWM (cont.)						
	D_{MAX} input current	D_{MAX} = 0.5V			-1	µA
	D_{MAX} threshold		0.95	1.06	1.17	V
Power Supply						
	I_{SUPPLY} static	V_{CC} = 12.7V	9		18	mA
V_{CC}	Supply voltage		9.3		14	V
V_{REF}	Reference voltage	TRIMMED VALUE		7.42		V
	V_{REF} tolerance	0 to 85°C			±3.5	%
	V_{REF} load current				-5	mA
	I_{REF} short circuit current	V_{REF} = 0V		-30		mA
Buffer						
	OUT_P / OUT_H LOW	IPC = 40mA			1	V
		IPC = 250mA PULSE			3	
	OUT_P / OUT_H HIGH	IPC = -40mA	10.2			
		IPC = -250mA PULSE	8.1			
	OUT_P / OUT_H peak triangle wave current	Magnetizing			±40	mA
	OUT_P / OUT_H pulse current	Gate capacitance current			±250	mA
	Low supply upper trip point		10.45	11.0	11.55	V
	Low supply lower trip point		9.5	10.0	10.5	V
Lamp Voltage Regulator						
	V_{LAMP} input current	V_{LAMP} = 6.5V			-8	µA
	V_{LAMP} threshold		7.05	7.42	7.79	V
Load Protection						
	I_{PRIM} input current	I_{PRIM} = 0V	-60	-100	-140	µA
	I_{PRIM} negative threshold		-60	-100	-140	mV
Over-current Protection						
	CSI input current	CSI = -1V	-60	-100	-140	µA
	CSI threshold		-400	-500	-650	mV
Rectifier (RLi = RLi2 = 4k, R_3 = 20k; VRLi = Voltage input to RLi1; VRLi2 = 0V, Input to RLi2)						
	Li input current	VRLi1 = VRLi2 = 0V	-120	-200	-280	µA
	C_{RECT} output offset	VRLi1 = VRLi2 = 0V			150	mV
	C_{RECT} HIGH output	VRLi1 = ±0.5V	4.42	4.66	4.9	V
	C_{RECT} gain	V_{RECT}/VRLi1	8.86	9.33	9.80	
	C_{RECT} error amp reference		2.01	2.12	2.23	V

DIP20: plastic dual in-line package; 20 leads (300 mil) **SOT146-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D [1]	E [1]	e	e_1	L	M_E	M_H	w	Z [1] max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.42 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.2	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.040 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			92-11-17 95-05-24