Data Sheet | September 1998 | File Number 2906.4

8.5MHz, Ultra-Low Noise Precision Operational Amplifier

The HA-5127 monolithic operational amplifier features an unparalleled combination of precision DC and wideband high speed characteristics. Utilizing the Intersil D. I. technology and advanced processing techniques, this unique design unites low noise (3nV/$\sqrt{Hz}$) precision instrumentation performance with high speed (10V/µs) wideband capability.

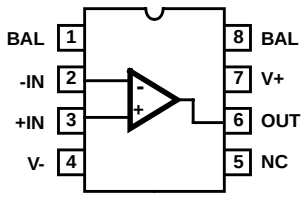
This amplifier's impressive list of features include low V_{OS} (10µV), wide unity gain-bandwidth (8.5MHz), high open loop gain (1800V/mV), and high CMRR (126dB). Additionally, this flexible device operates over a wide supply range (±5V to ±15V) while consuming only 140mW of power.

Using the HA-5127 allows designers to minimize errors while maximizing speed and bandwidth.

This device is ideally suited for low level transducer signal amplifier circuits. Other applications which can utilize the HA-5127's qualities include instrumentation amplifiers, pulse amplifiers, audio preamplifiers, and signal conditioning circuits. This device can easily be used as a design enhancement by directly replacing the 725, OP25, OP06, OP07, OP27 and OP37. For the military grade product, refer to the HA-5127/883 data sheet.

Pinout

HA-5127
(CERDIP, SOIC)
TOP VIEW



Features

- Slew Rate 10V/µs
- Unity Gain Bandwidth 8.5MHz
- Low Noise . . . . . 3nV/$\sqrt{Hz}$ at 1kHz
- Low V_{OS} 10µV
- High CMRR 126dB
- High Gain 1800V/mV

Applications

- High Speed Signal Conditioners
- Wide Bandwidth Instrumentation Amplifiers
- Low Level Transducer Amplifiers
- Fast, Low Level Voltage Comparators
- Highest Quality Audio Preamplifiers
- Pulse/RF Amplifiers

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
HA7-5127-2	-55 to 125	8 Ld CERDIP	F8.3A
HA7-5127-5	0 to 75	8 Ld CERDIP	F8.3A
HA7-5127A-5	0 to 75	8 Ld CERDIP	F8.3A
HA9P5127-5 (H51275)	0 to 75	8 Ld SOIC	M8.15

Absolute Maximum Ratings

Supply Voltage Between V+ and V- Terminals 44V
Differential Input Voltage (Note 3) 0.7V
Output Current . . . . . Full Short Circuit Protection

Operating Conditions

Temperature Range
HA-5127-2 . . . . . -55^oC to 125^oC
HA5127/27A-5 . . . . . 0^oC to 75^oC

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
CERDIP Package	135	50
SOIC Package	157	N/A

Maximum Junction Temperature (Ceramic Package, Note 1) . . . 175^oC
Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Maximum power dissipation, including output load must be designed to maintain the maximum junction temperature below 175^oC for Hermetic packages, and below 150^oC for the plastic packages.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
3. For differential input voltages greater than 0.7V, the input current must be limited to 25mA to protect the back-to-back input diodes.

Electrical Specifications $V_{SUPPLY} = \pm15V$, $C_L < 50pF$, $R_S < 100\Omega$

PARAMETER	TEST CONDITIONS	TEMP. (^oC)	HA-5127A			HA-5127			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS									
Offset Voltage		25	-	10	25	-	30	100	µV
		Full	-	30	60	-	70	300	µV
Average Offset Voltage Drift		Full	-	0.2	0.6	-	0.4	1.8	µV/^oC
Bias Current		25	-	±10	±40	-	±15	±80	nA
		Full	-	±20	±60	-	±35	±150	nA
Offset Current		25	-	7	35	-	12	75	nA
		Full	-	15	50	-	30	135	nA
Common Mode Range		Full	±10.3	±11.5	-	±10.3	±11.5	-	V
Differential Input Resistance (Note 4)		25	1.5	6	-	0.8	4	-	MΩ
Input Noise Voltage (Note 5)	0.1Hz to 10Hz	25	-	0.08	0.18	-	0.09	0.25	μV_{P-P}
Input Noise Voltage Density (Note 6)	f = 10Hz	25	-	3.5	8.0	-	3.8	8.0	nV/$\sqrt{Hz}$
	f = 100Hz		-	3.1	4.5	-	3.3	4.5	nV/$\sqrt{Hz}$
	f = 1000Hz		-	3.0	3.8	-	3.2	3.8	nV/$\sqrt{Hz}$
Input Noise Current Density (Note 6)	f = 10Hz	25	-	1.7	4.0	-	1.7	-	pA/$\sqrt{Hz}$
	f = 100Hz		-	1.0	2.3	-	1.0	-	pA/$\sqrt{Hz}$
	f = 1000Hz		-	0.4	0.6	-	0.4	0.6	pA/$\sqrt{Hz}$
TRANSFER CHARACTERISTICS									
Large Signal Voltage Gain	$V_{OUT} = \pm10V$, $R_L = 2k\Omega$	25	1000	1800	-	700	1500	-	V/mV
		Full	600	1200	-	300	800	-	V/mV
Common Mode Rejection Ratio	$V_{CM} = \pm10V$	Full	114	126	-	100	120	-	dB
Minimum Stable Gain		25	1	-	-	1	-	-	V/V
Unity-Gain-Bandwidth		25	5	8.5	-	5	8.5	-	MHz
OUTPUT CHARACTERISTICS									
Output Voltage Swing	$R_L = 600\Omega$	25	±10.0	±11.5	-	±10.0	±11.5	-	V
	$R_L = 2k\Omega$	Full	±11.7	±13.8	-	±11.5	±13.5	-	V
Full Power Bandwidth (Note 7)		25	111	160	-	111	160	-	kHz
Output Resistance	Open Loop	25	-	70	-	-	70	-	Ω
Output Current		25	16.5	25	-	16.5	25	-	mA
TRANSIENT RESPONSE (Note 8)									
Rise Time		25	-	-	150	-	-	150	ns

Electrical Specifications $V_{SUPPLY} = \pm15V$, $C_L < 50pF$, $R_S < 100\Omega$ **(Continued)**

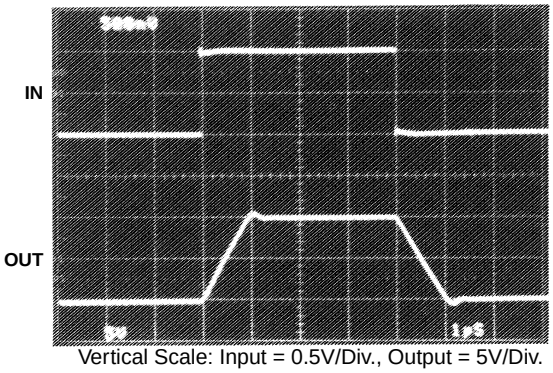
PARAMETER	TEST CONDITIONS	TEMP. (^oC)	HA-5127A			HA-5127			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Slew Rate	V_{OUT} = 10V	25	7	10	-	7	10	-	V/µs
Settling Time (Note 9)		25	-	1.5	-	-	1.5	-	µs
Overshoot		25	-	20	40	-	20	40	%
POWER SUPPLY CHARACTERISTICS									
Supply Current		25	-	3.5	-	-	3.5	-	mA
		Full	-	-	4.0	-	-	4.0	mA
Power Supply Rejection Ratio	$V_S = \pm4.5V$ to $\pm18V$	Full	-	2	4	-	16	51	µV/V

NOTES:

4. This parameter value is based upon design calculations.
5. Refer to Typical Performance Curves.
6. The limits for this parameter are guaranteed based on lab characterization, and reflect lot-to-lot variation.
7. Full power bandwidth guaranteed based on slew rate measurement using: $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$.
8. Refer to Test Circuits section of the data sheet.
9. Settling time is specified to 0.1% of final value for a 10V output step and $A_V = -1$.

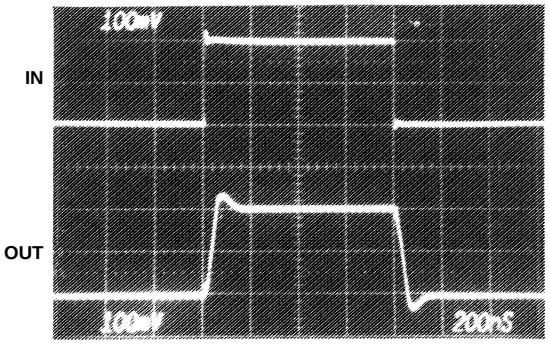
Test Circuits and Waveforms

FIGURE 1. LARGE AND SMALL SIGNAL RESPONSE TEST CIRCUITS



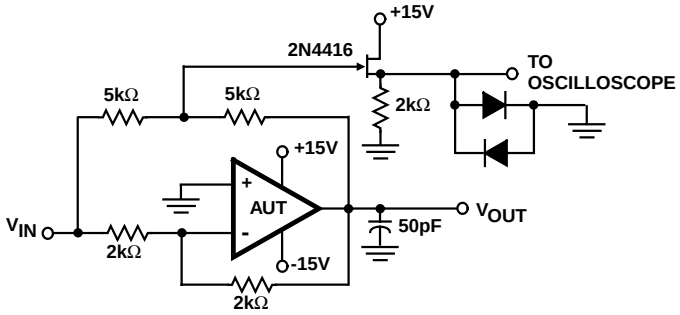
Vertical Scale: Input = 0.5V/Div., Output = 5V/Div.
Horizontal Scale: 1µs/Div.

LARGE SIGNAL RESPONSE



Vertical Scale: 100mV/Div.
Horizontal Scale: 200ns/Div.

SMALL SIGNAL RESPONSE

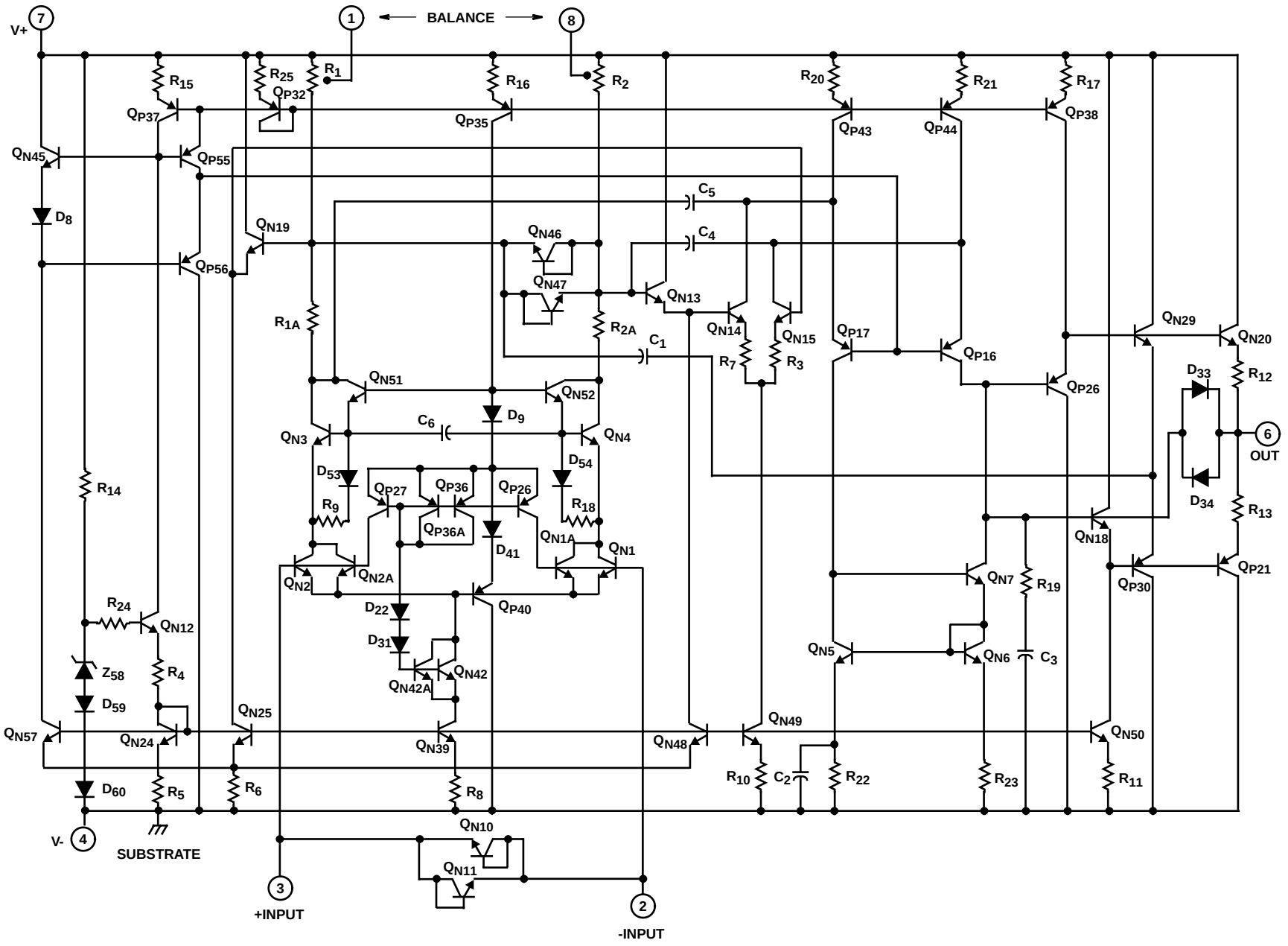


NOTES:

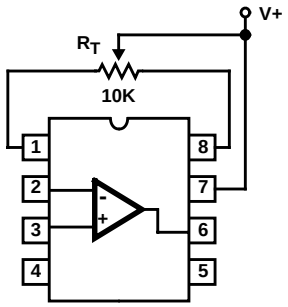
10. $A_V = -1$.
11. Feedback and summing resistors should be 0.1% matched.
12. Clipping diodes are optional. HP5082-2810 recommended.

FIGURE 2. SETTLING TIME TEST CIRCUIT

Schematic Diagram



Application Information



NOTE: Tested Offset Adjustment Range is $|V_{OS} + 1mV|$ minimum referred to output. Typical range is ±4mV with $R_T = 10k\Omega$.

FIGURE 3. SUGGESTED OFFSET VOLTAGE ADJUSTMENT

Low resistances are preferred for low noise applications as a 1kΩ resistor has $4nV/\sqrt{Hz}$ of thermal noise. Total resistances of greater than 10kΩ on either input can reduce stability. In most high resistance applications, a few picofarads of capacitance across the feedback resistor will improve stability.

FIGURE 4. SUGGESTED STABILITY CIRCUITS

Typical Performance Curves

Unless Otherwise Specified: $T_A = 25^oC$, $V_{SUPPLY} = \pm 15V$

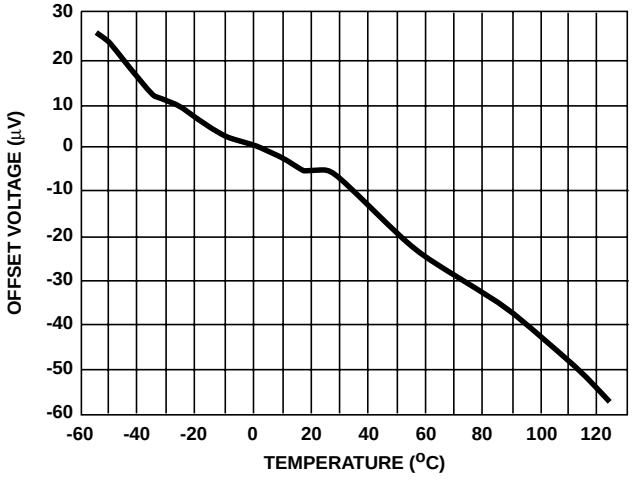


FIGURE 5. TYPICAL OFFSET VOLTAGE DRIFT vs TEMPERATURE

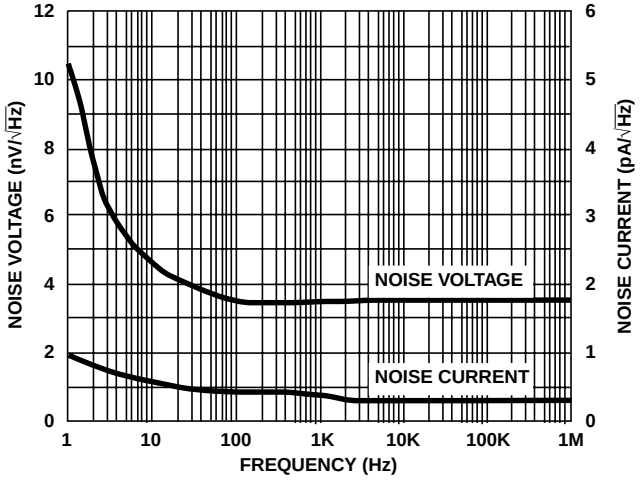


FIGURE 6. NOISE CHARACTERISTICS

Typical Performance Curves Unless Otherwise Specified: $T_A = 25^oC$, $V_{SUPPLY} = \pm 15V$ **(Continued)**

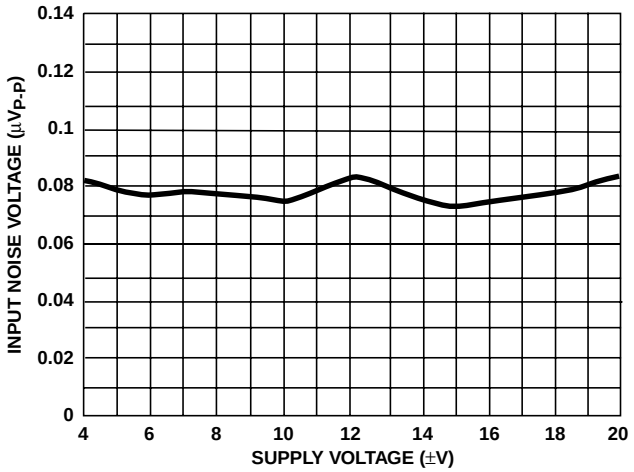


FIGURE 7. NOISE vs SUPPLY VOLTAGE

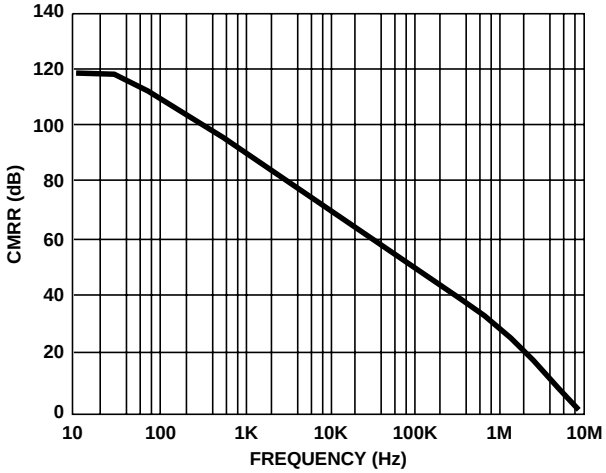


FIGURE 8. CMRR vs FREQUENCY

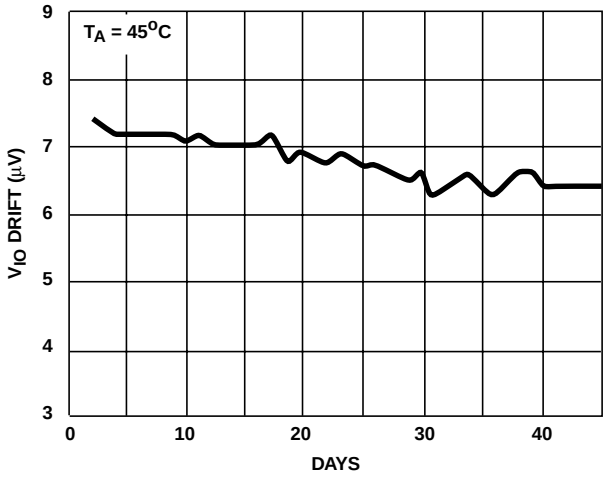


FIGURE 9. OFFSET VOLTAGE DRIFT vs TIME

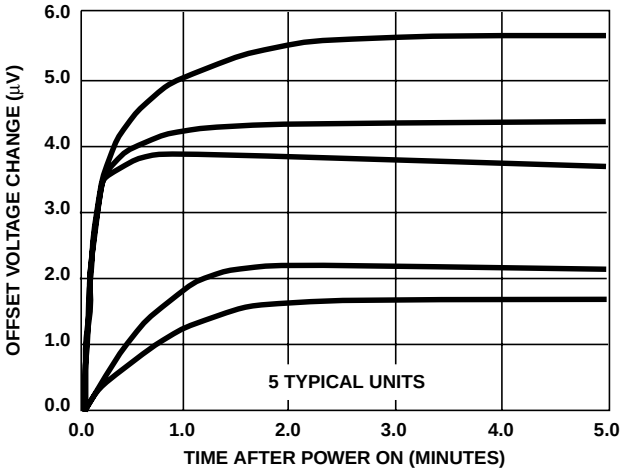


FIGURE 10. OFFSET VOLTAGE WARM UP DRIFT

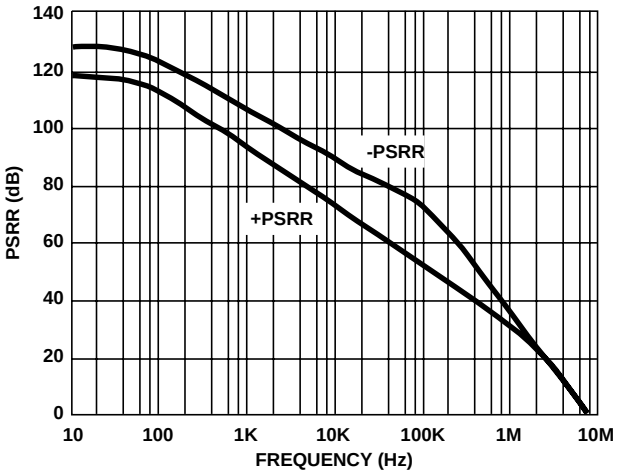


FIGURE 11. PSRR vs FREQUENCY

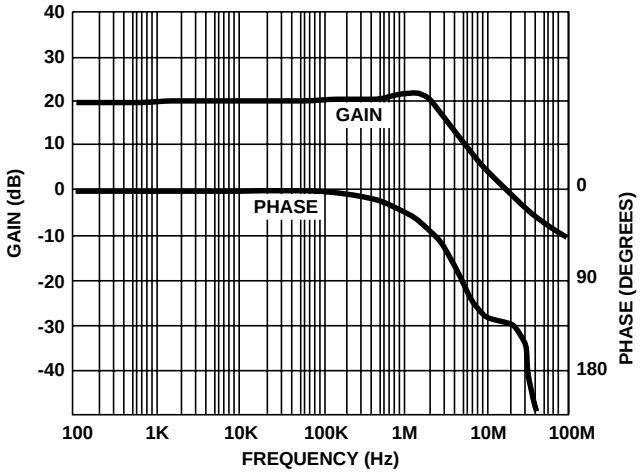


FIGURE 12. CLOSED LOOP GAIN AND PHASE vs FREQUENCY

Typical Performance Curves Unless Otherwise Specified: $T_A = 25^oC$, $V_{SUPPLY} = \pm 15V$ **(Continued)**

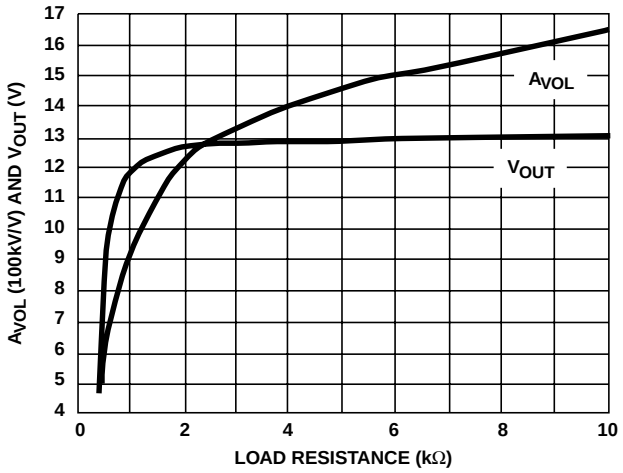


FIGURE 13. A_{VOL} AND V_{OUT} vs LOAD RESISTANCE

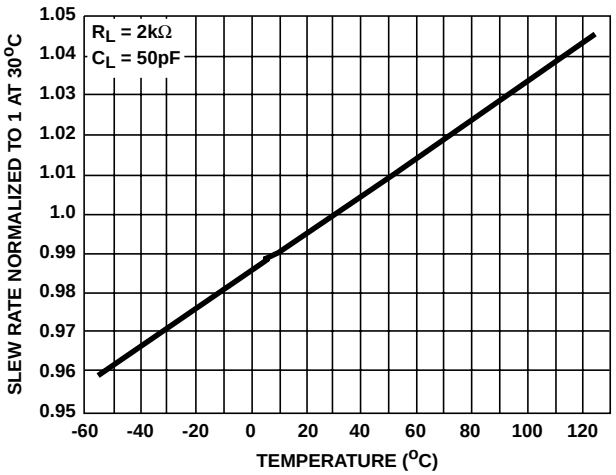


FIGURE 14. NORMALIZED SLEW RATE vs TEMPERATURE

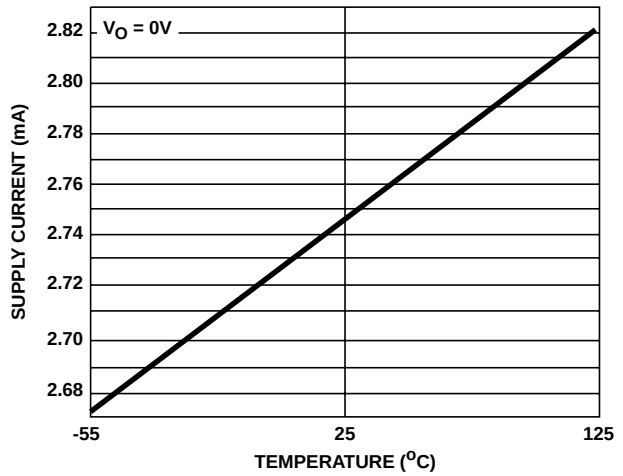


FIGURE 15. SUPPLY CURRENT vs TEMPERATURE

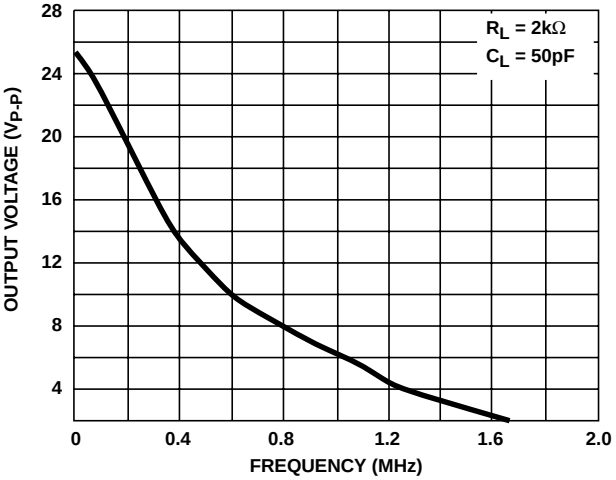


FIGURE 16. MAX UNDISTORTED SINEWAVE OUTPUT vs FREQUENCY

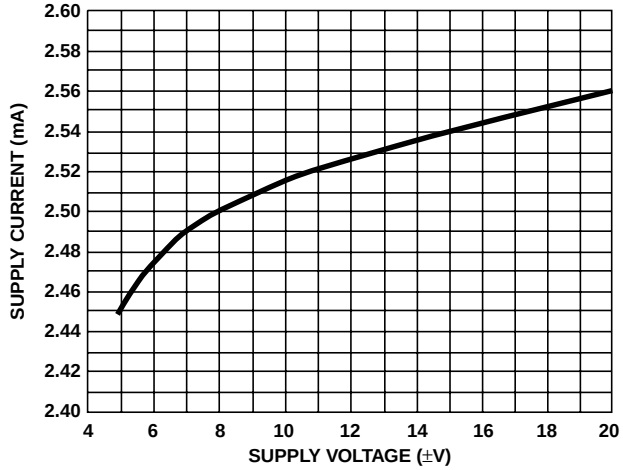


FIGURE 17. SUPPLY CURRENT vs SUPPLY VOLTAGE

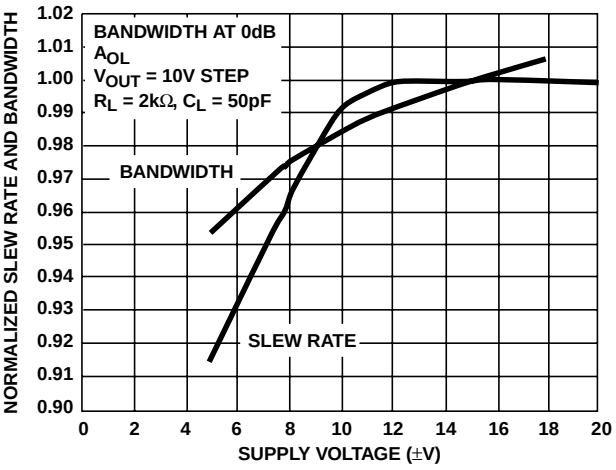


FIGURE 18. BANDWIDTH AND SLEW RATE vs SUPPLY VOLTAGE

Typical Performance Curves Unless Otherwise Specified: $T_A = 25^oC$, $V_{SUPPLY} = \pm 15V$ **(Continued)**

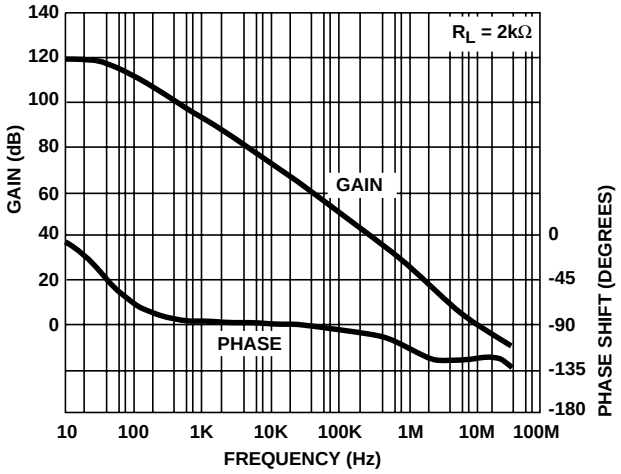


FIGURE 19. OPEN LOOP GAIN AND PHASE

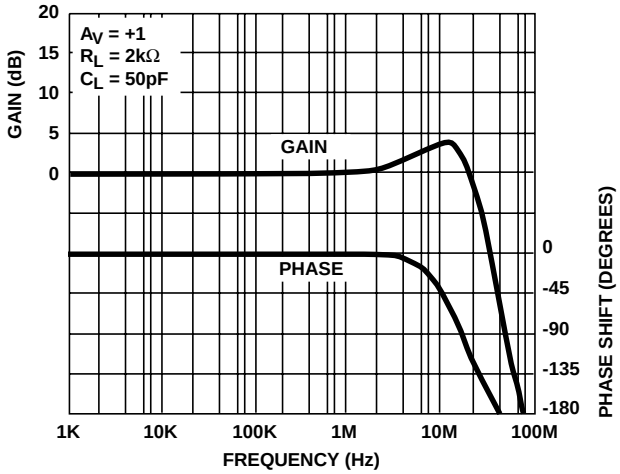
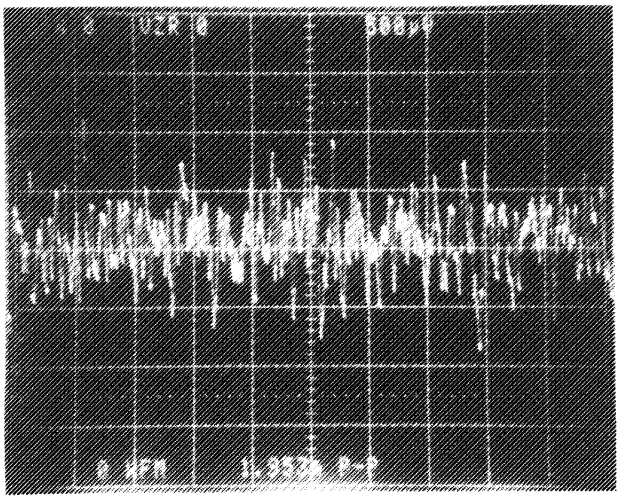


FIGURE 20. CLOSED LOOP GAIN AND PHASE



Horizontal Scale = 1s/Div.
Vertical Scale = 0.002µV/Div.
A_{CL} = 25,000V/V, E_N = 0.08μV_{P-P} RTI

FIGURE 21. PEAK-TO-PEAK NOISE VOLTAGE (0.1Hz TO 10Hz)

Die Characteristics

DIE DIMENSIONS:

104 mils x 65 mils x 19 mils
2650µm x 1650µm x 483µm

METALLIZATION:

Type: Al, 1% Cu
Thickness: 16kÅ ±2kÅ

SUBSTRATE POTENTIAL (Powered Up):

V-

PASSIVATION:

Type: Nitride (Si_3N_4) over Silox (SiO_2, 5% Phos.)
Silox Thickness: 12kÅ ±2kÅ
Nitride Thickness: 3.5kÅ ±1.5kÅ

TRANSISTOR COUNT:

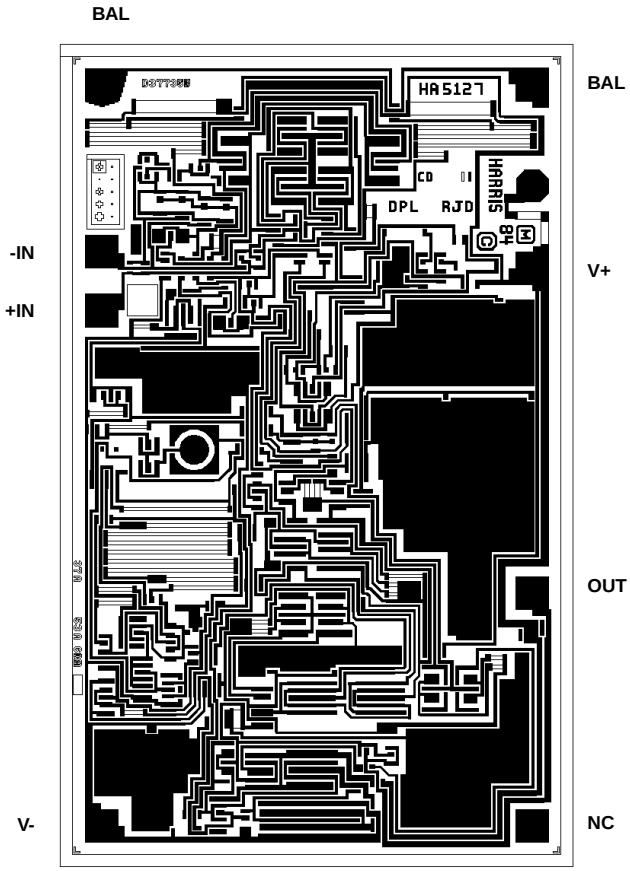
63

PROCESS:

Bipolar Dielectric Isolation

Metallization Mask Layout

HA-5127



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