G-LINK

GLT625608

32K x 8 SLOW SPEED CMOS STATIC RAM

Feb, 2004(Rev. 1.2)

Features :

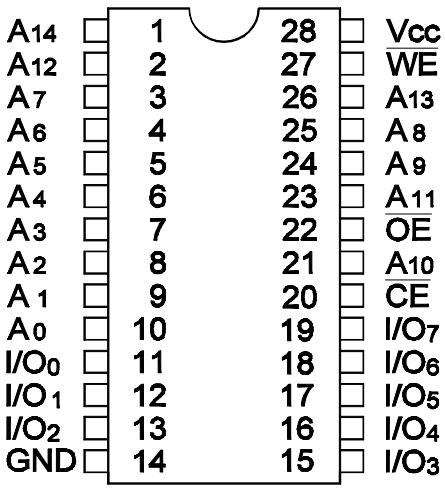
- Available in 70/100ns(MAX.)
- Automatic power-down when chip disabled
- Low power consumption:
  GLT625608
  -467.5mW(Max.) Operating
- -500μW(Max.)Standby
- TTL compatible interface levels
- Single 5V power supply
- Fully static operation
- Three state outputs
- 256K bit EPROM pin compatible
- Data Retention as low as 2V
- Industrial Grade (-40°C~85°C) available.

Description :

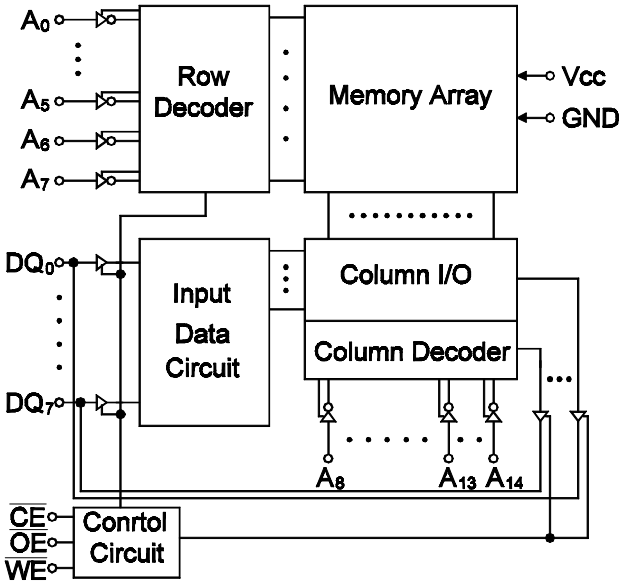
GLT625608 is a 262,144-bit static random access memory organized as 32,768 words by 8 bits and operates from a single 5 volt supply. Inputs and three-state outputs are TTL compatible and allow for direct interfacing with system I/O bus. The GLT625608 is available in a standard 330 mil SOP packages. Other packages will also available upon request.

Pin Configurations:

GLT625608



Function Block Diagram :



Pin Descriptions:

Name	Function
A_0 - A_{14}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$\overline{CE}$	Chip Enable
I/O_0-I/O_7	Data Input/Output
V_{cc}	Power Supply (+5V)
GND	Ground

Truth Table:

Mode	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	I/O Operation	Supply Current
Not Selected	X	H	X	High Z	I_{SB},I_{SB1}
(Power down)				High Z	I_{SB},I_{SB1}
Output Disabled	H	L	H	High Z	I_{CC}
Read	H	L	L	D_{OUT}	I_{CC}
Write	L	L	X	D_{IN}	I_{CC}

NOTE: X : H or L

Absolute Maximum Ratings:

Ambient Temperature
Under Bias.....-10°C to +80°C
Storage Temperature(plastic)....-55°C to +125°C
Voltage Relative to GND.....-0.5V to + 7.0V
Data Output Current.....50mA
Power Dissipation.....1.0W

1.Stresses greater than those listed under ABSOLUTE MAXIMUM RATING may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operation Range :

RANGE	AMBIENT TEMPERATURE	Vcc
Commercial	0°C to + 70°C	5V ± 10%
Industrial	-40°C to 85°C	5V ± 10%

Capaccitance[(1)](T_A=25°C,F=1.0MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
CIN	Input Capacitance	VIN=0V	6	pF
CDQ	Input/Output capacitance	VI/O=0	8	pF

1.This parameter is guaranteed and tested.

DC Characteristics

Sym.	Parameter	Test Conditions	Min.	Typ[1]	Max.	Unit
V_{IL}	Guaranteed Input Low Voltage [2][3]		-0.3	-	+0.8	V
V_{IH}	Guaranteed Input High Voltage [2]		2.2	-	V_{CC}+0.3	V
I_{LI}	Input Leakage Current	V_{CC}=Max., V_{IN}=0V to V_{CC}	-5	-	5	μA
I_{LO}	Output Leakage Current	V_{CC}=Max., $\overline{CE} \geq V_{IH}$	-5	-	5	μA
V_{OL}	Output Low Voltage	V_{CC}=Min., I_{OL} =8mA	-	-	0.4	V
V_{OH}	Output High Voltage	V_{CC}=Min., I_{OH} =-4mA	2.4	-	-	V
I_{CC}	Operating Power Supply Current	V_{CC}=Max., $\overline{CE} \leq V_{IL}$, $I_{I/O}$=0mA., F=F_{max}[3]	-	-	100	mA
I_{CCSB}	Standby Power Supply Current	V_{CC}=Max., $\overline{CE} \geq V_{IH}$, $I_{I/O}$=0mA., F=F_{max}[3]	-	-	20	mA
I_{CCSB1}	Power Down Power Supply Current	V_{CC}=Max., $\overline{CE} \geq V_{CC}$.-0.2V, $V_{IN} \geq V_{CC}$. -0.2V or	-	10	10	mA

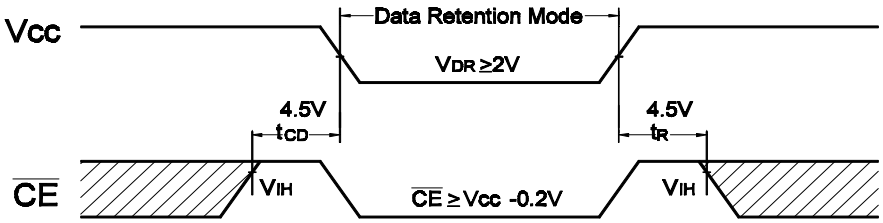
1. Typical characteristics are at V_{CC}=5V, T_A=25°C.
2. These are absolute values with repeat to device ground and all overshoots due to system or tester noise are included.
3. $F_{MAX}=1/t_{RC}$.

Data Retention

Sym.	Parameter	Test Conditions	Min.	Typ	Max.	Unit
V_{DR}	V_{CC} for Data retention	$\overline{CE} \geq V_{CC}$ -0.2V $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq 0.2V$	2.0	-	-	V
I_{CCDR}	Data Retention Current	$\overline{CE} \geq V_{DR}$ - 0.2V $V_{IN} \geq V_{DR}$ - 0.2V or $V_{IN} \leq 0.2V$	-	2	50	μA[1]
t_{CDR}	Chip Deselect to Data Retention Time	See Retention Waveform	0	-	-	ns
t_R	Operating Recovery Time		t_{RC}[2]	-	-	ns

1. V_{DR} = 3V, T_A = Specified
2. t_{RC} = Read Cycle Time

Low V_{CC} Data Retention Waveform ($\overline{CE}$ Controlled)



AC Test Conditions

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Level	1.5V

AC Test Loads and Waveforms

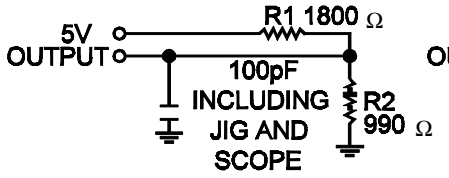


Figure 1a

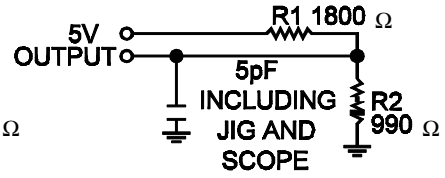


Figure 1b

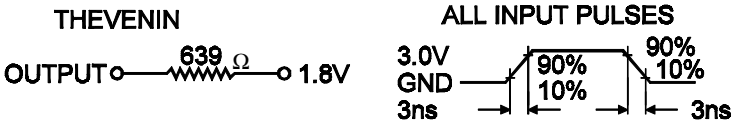


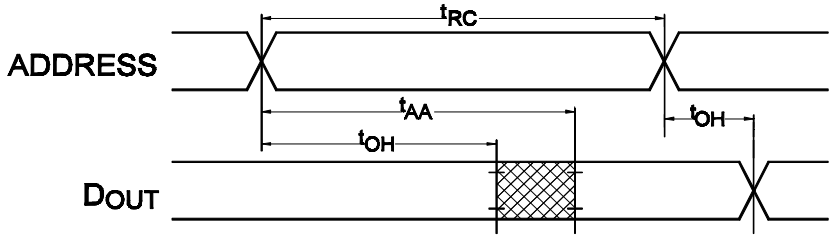
Figure 2

AC Electrical Characteristics
Read Cycle

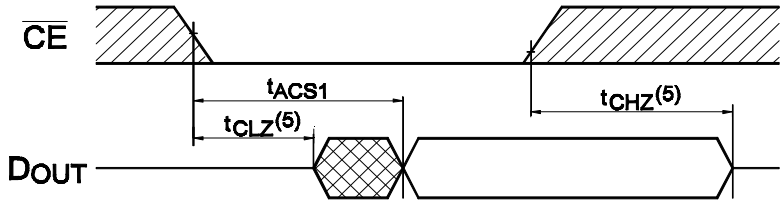
JEDEC Parameter Name	Parameter Name	Parameter	625608-70		625608-10		Unit
			Min.	Max.	Min.	Max.	
t_{AVAX}	t_{RC}	Read Cycle Time	70	-	100	-	ns
t_{AVQV}	t_{AA}	Address Access Time	-	70	-	100	ns
t_{ELQV}	t_{ACS}	Chip Select Access Time	-	70	-	100	ns
t_{GLQV}	t_{OE}	Output Enable to Output Valid	-	40	-	50	ns
t_{ELQZ}	t_{CLZ}	Chip Deselect to Output in Low Z	5	-	10	-	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z	5	-	5	-	ns
t_{EHQZ}	t_{CHZ}	Chip Deselect to Output in High Z	0	30	0	35	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z	0	30	0	35	ns
t_{AXQX}	t_{OH}	Output Hold from Address Change	5	-	10	-	ns

Switching Waveforms (Read Cycle)

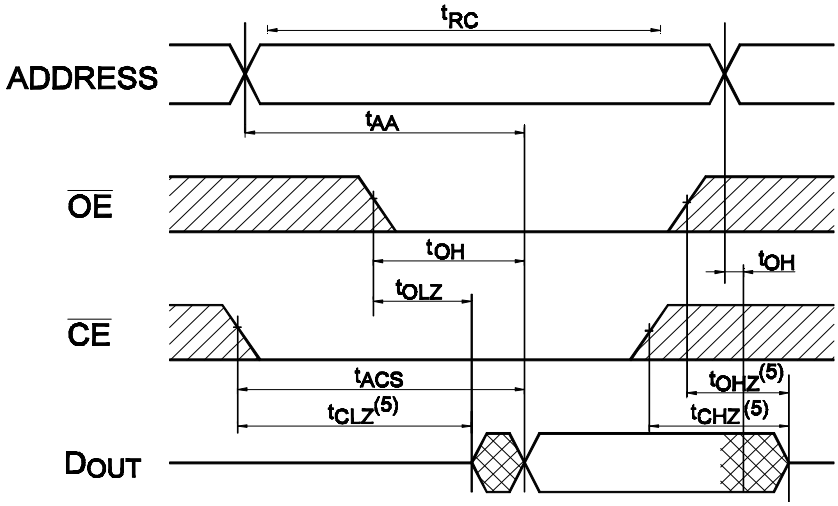
READ CYCLE 1[1,2,4]



READ CYCLE 2[1,3,4]



READ CYCLE 3[1]



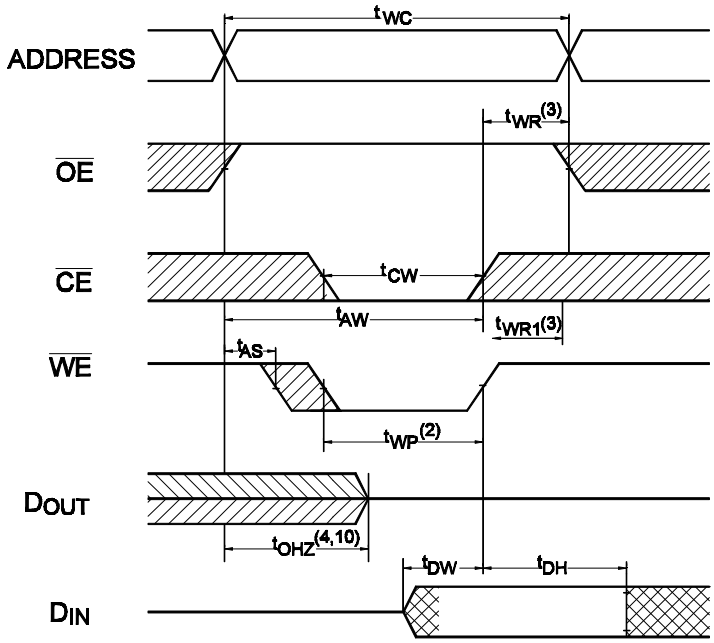
Notes:

1. **WE** is High for READ Cycle.
2. Device is continuously selected **OE** = V_{IL}.
3. Address valid prior to or coincident with **CE** transition low.
4. **CE** = V_{IL}.
5. Transition is measured ±500mV from steady state with C_L = 5pF as shown in Figure 1b. This parameter is guaranteed but not 100% tested.

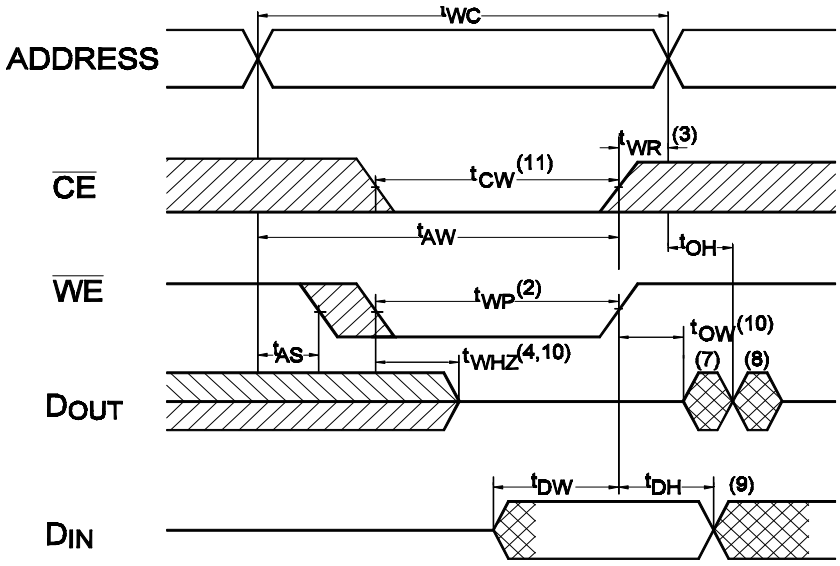
AC Electrical Characteristics
Write Cycle

JEDEC Parameter Name	Parameter Name	Parameter	625608-70		625608-10		Unit
			Min.	Max.	Min.	Max.	
t_{AVAX}	t_{WC}	Write Cycle Time	70	-	100	-	ns
t_{ELWH}	t_{CW}	Chip Enable to End of Write	65	-	90	-	ns
t_{AVWL}	t_{AS}	Address Set up Time	0	-	0	-	ns
t_{AVWH}	t_{AW}	Address Valid to End of Write	65	-	90	-	ns
t_{WLWH}	t_{WP}	Write Pulse Width	55	-	75	-	ns
t_{WHAX}	t_{WR1}	Write Recovery Time	5	-	5	-	ns
t_{WLQZ}	t_{WHZ}	Data to Write Time Overlap	0	30	0	35	ns
t_{DVWH}	t_{DW}	Data to Write Time Overlap	35	-	40	-	ns
t_{WHDX}	t_{DH}	Data Hold from Write Time	0	-	0	-	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z	0	30	0	40	ns
t_{WHQX}	t_{OW}	End of Write to Output Active	5	-	5	-	ns

Switching Waveforms (Write Cycle)
WRITE CYCLE 1[(1)]



WRITE CYCLE 2[1,6]



Note:

1. $\overline{WE}$ must be high during address transitions.
2. The internal write time of the memory is defined by the overlap of $\overline{CE}$ active and $\overline{WE}$ low. All signals must be active to initiate a write and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
3. T_{WR} is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high at the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE}$=V_{IL}).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\overline{CE}$ is low is high during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured ±200mV from steady state with C_L=5pF.
11. t_{CW} is measured from $\overline{CE}$ going low to the end of write.

Ordering Information

Part Number	*SPEED*	*POWER*	*PACKAGE*
GLT625608-10J3	10ns	Normal	SOJ 300mil 28L
GLT625608-70J3	70ns	Normal	SOJ 300mil 28L
GLT625608-10TS	10ns	Normal	TSOPI 28L
GLT625608-70TS	70ns	Normal	TSOPI 28L
GLT625608-10TC	10ns	Normal	TSOPII 28L
GLT625608-70TC	70ns	Normal	TSOPII 28L
GLT625608-10FB	10ns	Normal	SOP 330mil 28L
GLT625608-70FB	70ns	Normal	SOP 330mil 28L

Parts Numbers (Top Mark) Definition :

GLT 6 256 08 I - 10 TC

4 : DRAM
5 : Synchronous DRAM
6 : Standard SRAM /Pseudo SRAM
7 : Cache SRAM
8 : Synchronous Burst SRAM
9 : SGRAM

-SRAM
064 : 8K
256 : 256K
512 : 512K
100 : 1M
200 : 2M
400 : 4M

-DRAM
10 : 1M(C/EDO)
11 : 1M(C/FPM)
12 : 1M(H/EDO)
13 : 1M(H/FPM)
20 : 2M(EDO)
21 : 2M(FPM)
40 : 4M(EDO)
41 : 4M(FPM)
80 : 8M(EDO)
81 : 8M(FPM)
160 : 16M(EDO)
161 : 16M(FPM)
640 : 64M(EDO)
641 : 64M(FPM)

-SDRAM
40 : 4M
160 : 16M
320 : 32M,4Bank
640 : 64M
1280 : 128M

-PSEUDO SDRAM
020 – 2M
160 – 16M
320 – 32M

CONFIG.
04 : x04
08 : x08
16 : x16
32 : x32

VOLTAGE
Blank : 5V
L : 3.3V
M : 2.5V
N : 2.0V

POWER
Blank : Standard
L : Low Power
LL : Low Low Power
SL : Super Low Power

SPEED

-SRAM/PSEUDO SRAM
12 : 12ns
15 : 15ns
20 : 20ns
55 : 55ns
70 : 70ns
85 : 85ns
120 : 120ns

-DRAM
25 : 25ns
28 : 28ns
30 : 30ns
35 : 35ns
40 : 40ns
45 : 45ns
50 : 50ns
60 : 60ns
70 : 70ns
80 : 80ns
100 : 100ns

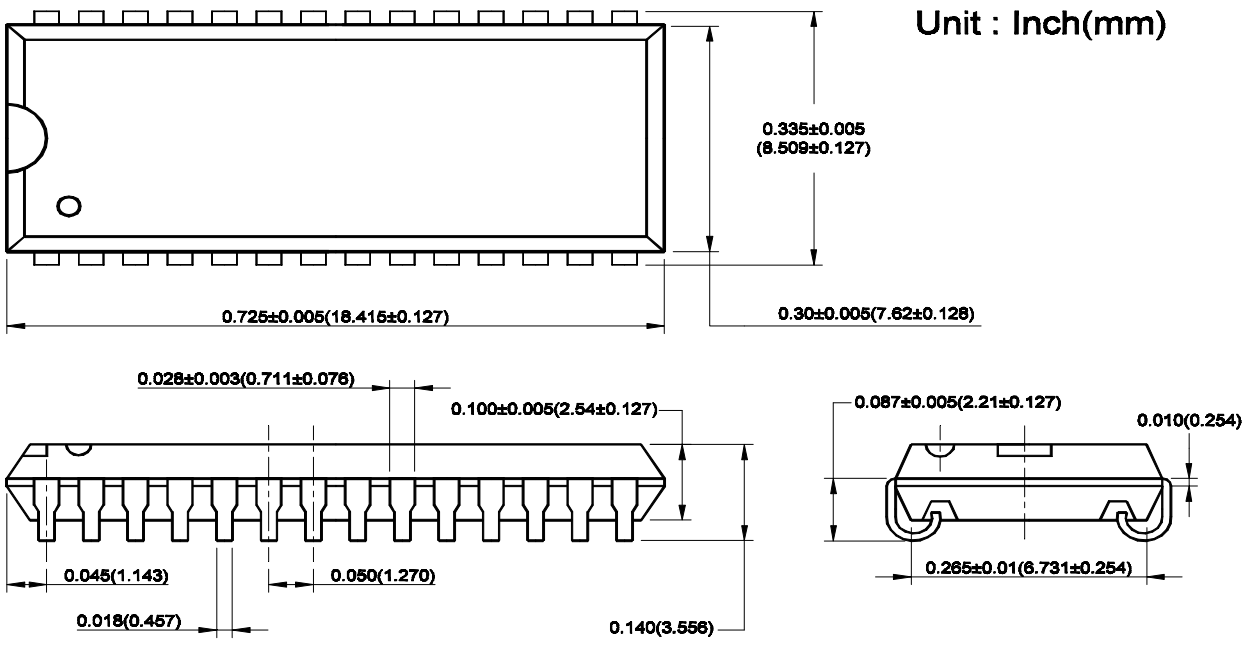
-SDRAM
5 : 5ns/200 MHZ
5.5 : 5.5ns/183 MHZ
6 : 6ns/166 MHZ
7 : 7ns/143 MHZ
8 : 8ns/125 MHZ
10 : 10ns/100 MHZ

PACKAGE
T : PDIP(300mil)
TS : TSOP(Type I)
ST : sTSOP(Type I)
TC : TSOPII (40/44)
PL : PLCC
FA : 300mil SOP
FB : 330mil SOP
FC : 445mil SOP
J3 : 300mil SOJ
J4 : 400mil SOJ
P : PDIP(600mil)
Q : PQFP
TQ : TQFP
FG : 48Pin BGA 9x12
FH : 48Pin BGA 8x10
FI : 48Pin BGA 6x8
FJ : 60Ball VFBGA

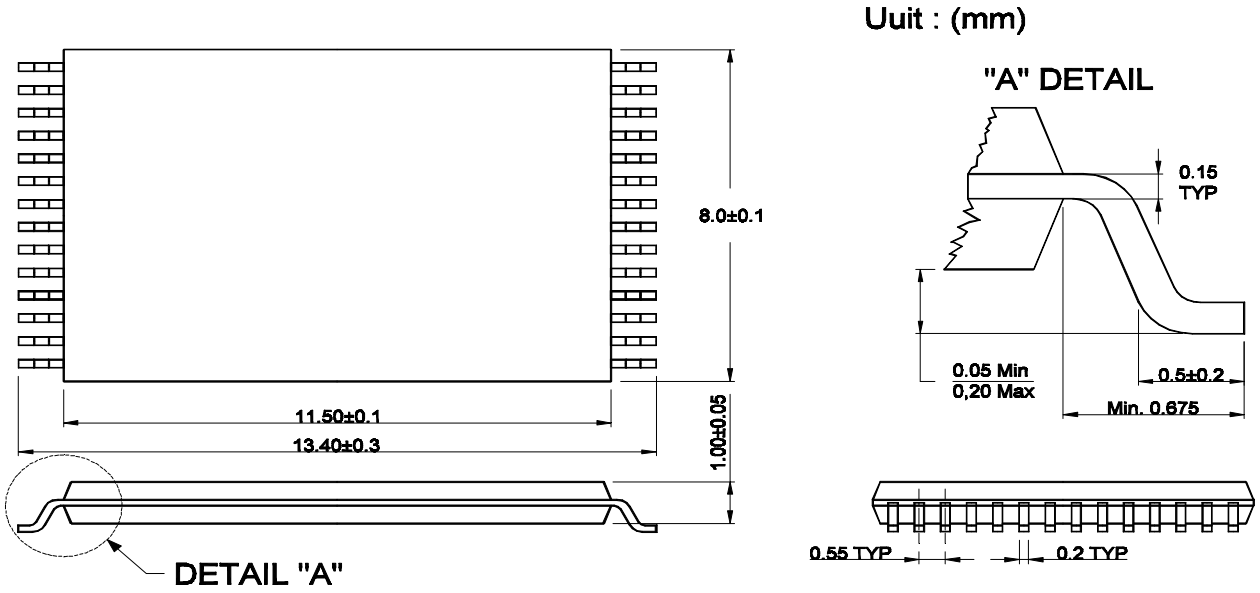
Temperature Range
E : Extended Temperature
II : Industrial Temperature
Blank : Commercial Temperature
P : Pb – free part

Package Information

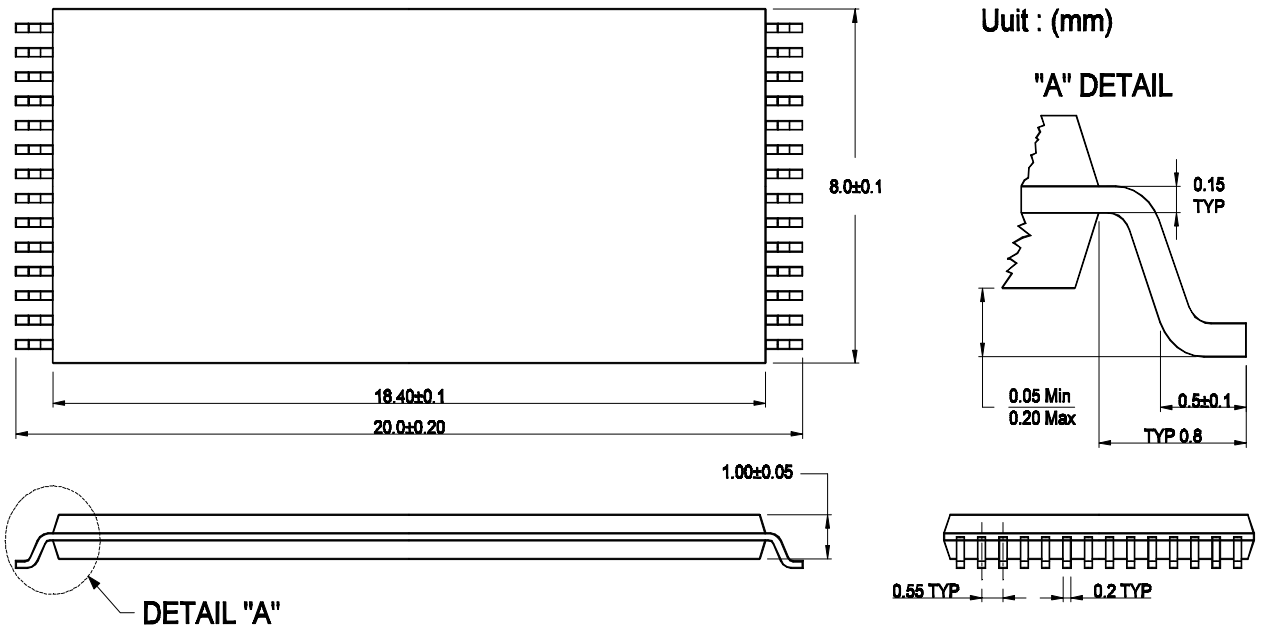
300mil 28 Lead Small Outline J-form Package (SOJ)



28 L (8 × 13.4 mm) Thin Small Outline Package (TSOP) Type I



28 L (8 × 20 mm) Thin Small Outline Package (TSOP) Type I



330mil 28 Lead Thin Small Outline(Gull-Wing) Package (SOP)